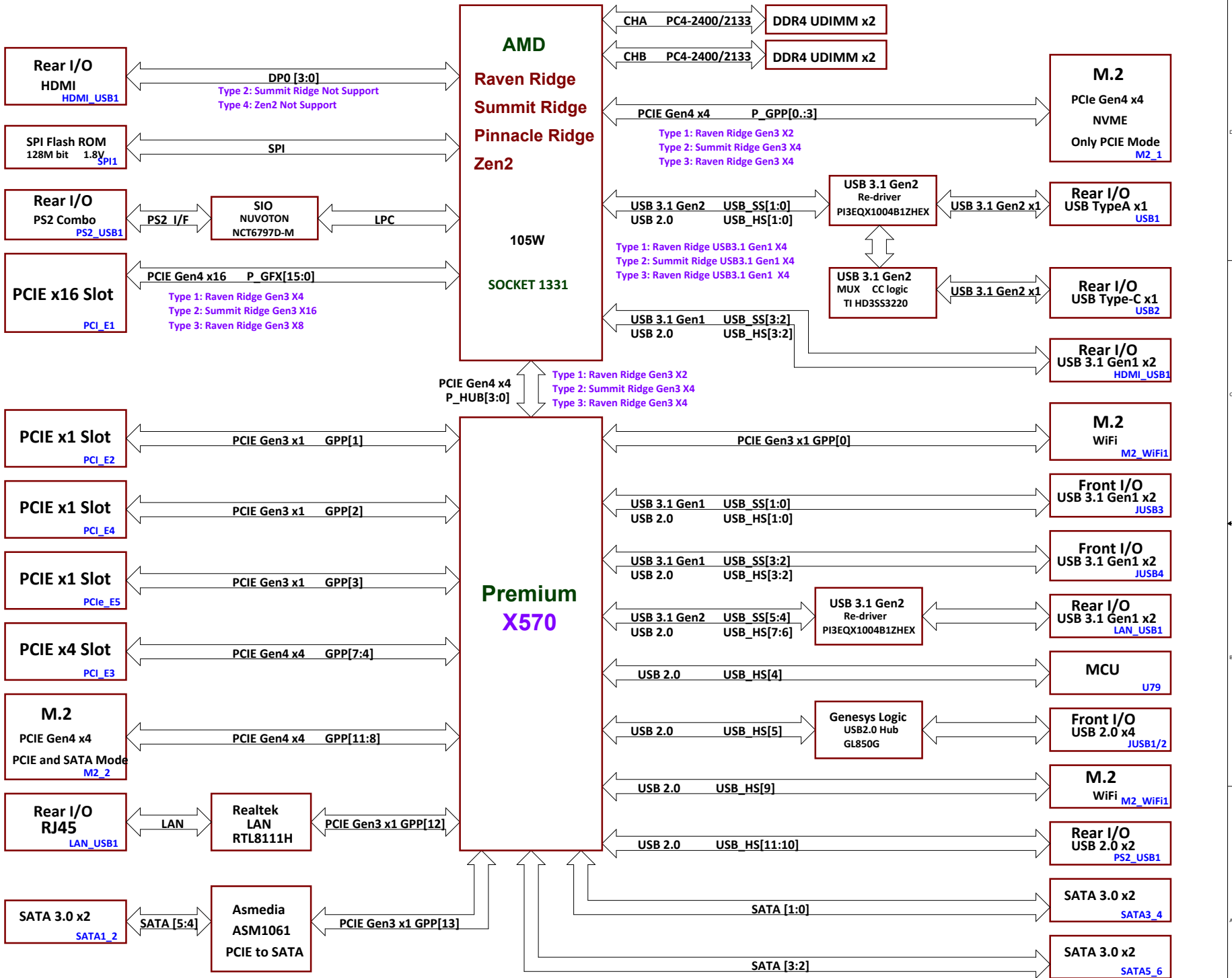
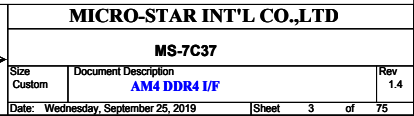
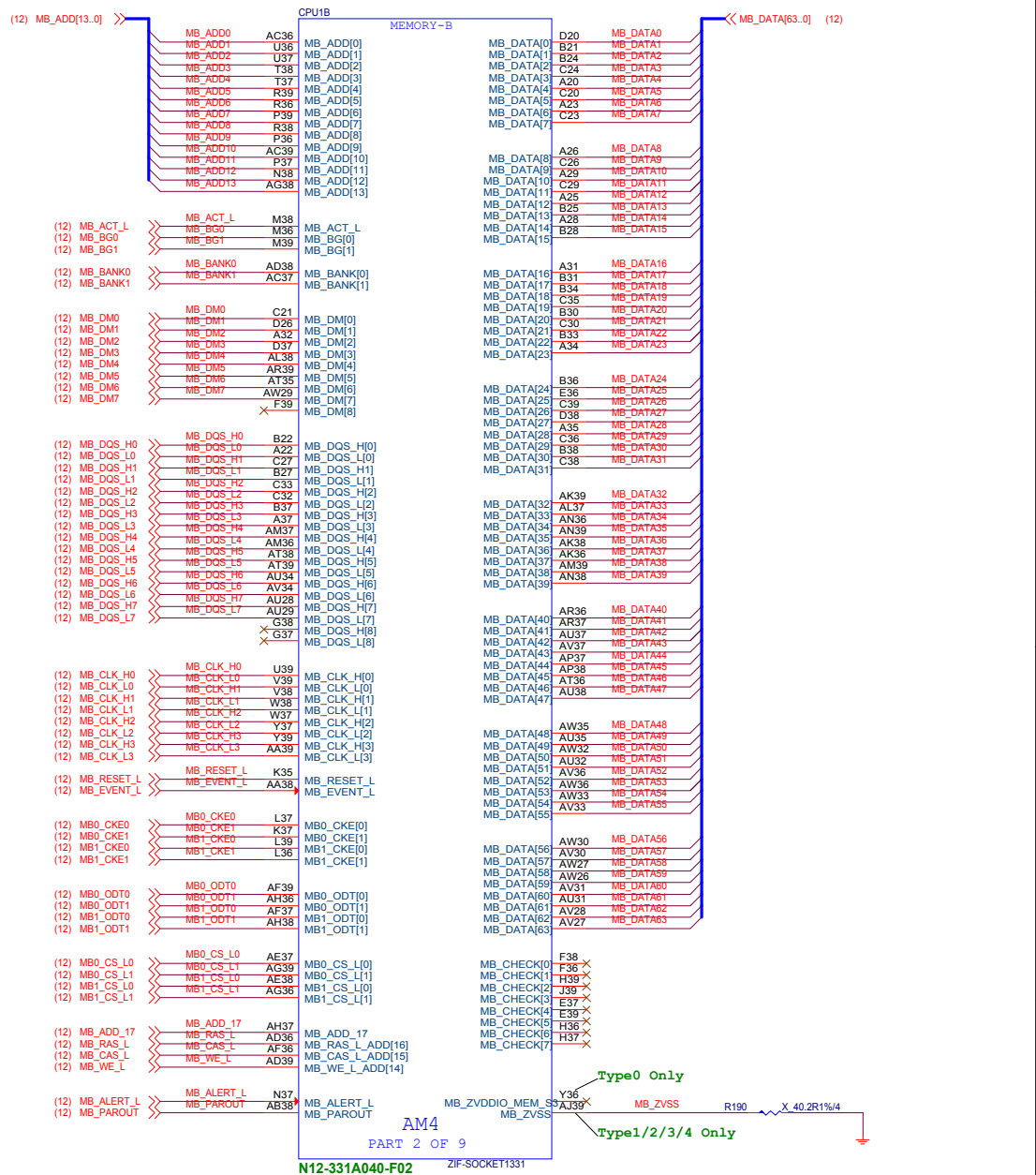


AMD AM4

GAMING EDGE AC

01	Cover Sheet	36	LAN - I211AT	66	MCU - LED Control
02	Block Diagram	37	Audio ALC1220P-VB	67	LED - Power / JPIPE
03	FM4 DDR4 I / F	38	Audio DePop	68	LED - JLED1 / 2 / 3 / 4
04	AM4 PCIE / SATAE	39	USB Power - UP7501	69	LED - Mystic Light - 1
05	AM4 Display / Audio	40	Front USB2.0 Header	70	LED - Mystic Light - 2
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07	AM4 LPC / SPI / USB / CLK / STRAP	42	Rear USB3.0 + PS2	72	Manual Parts
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21	PCI_E4 (X8)	51	CPU power NB 1-2		
22	PCIE Switch X16 / X8	52	CPU power NB_S5		
23	PCI_E1_E3_E5 (X1)	53	CPU power 1.8_S0 / S5		
24	PCI_E6 (X4)	54	CPU power VDDP - TPS56C215		
25	PCIE Switch X4 / M2_2	55	VRM PWRGD		
26	M.2_1	56	DDR Power - RT8125E		
27	M.2_2	57	DDR Power - VPP25 / VTT		
28	M.2_3 (WIFI+BT)	58	PROM - SY8288RAC / 1.05V		
29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrpntPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		



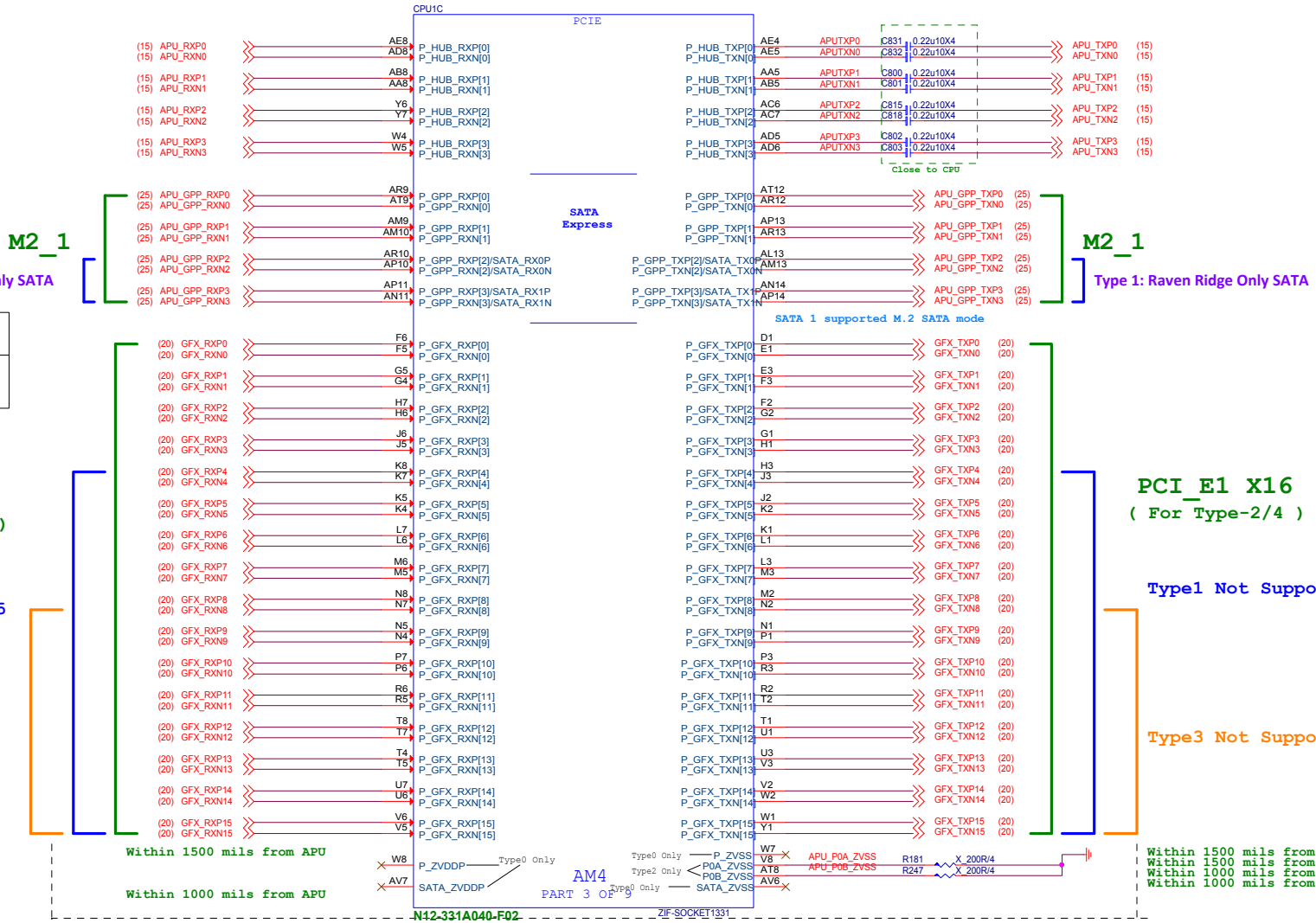


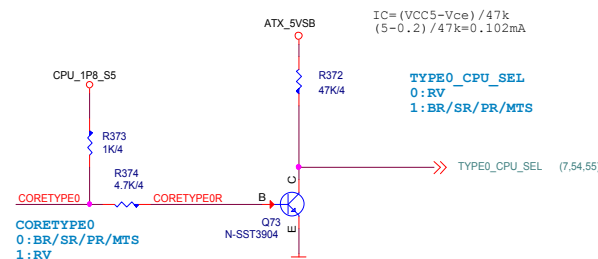
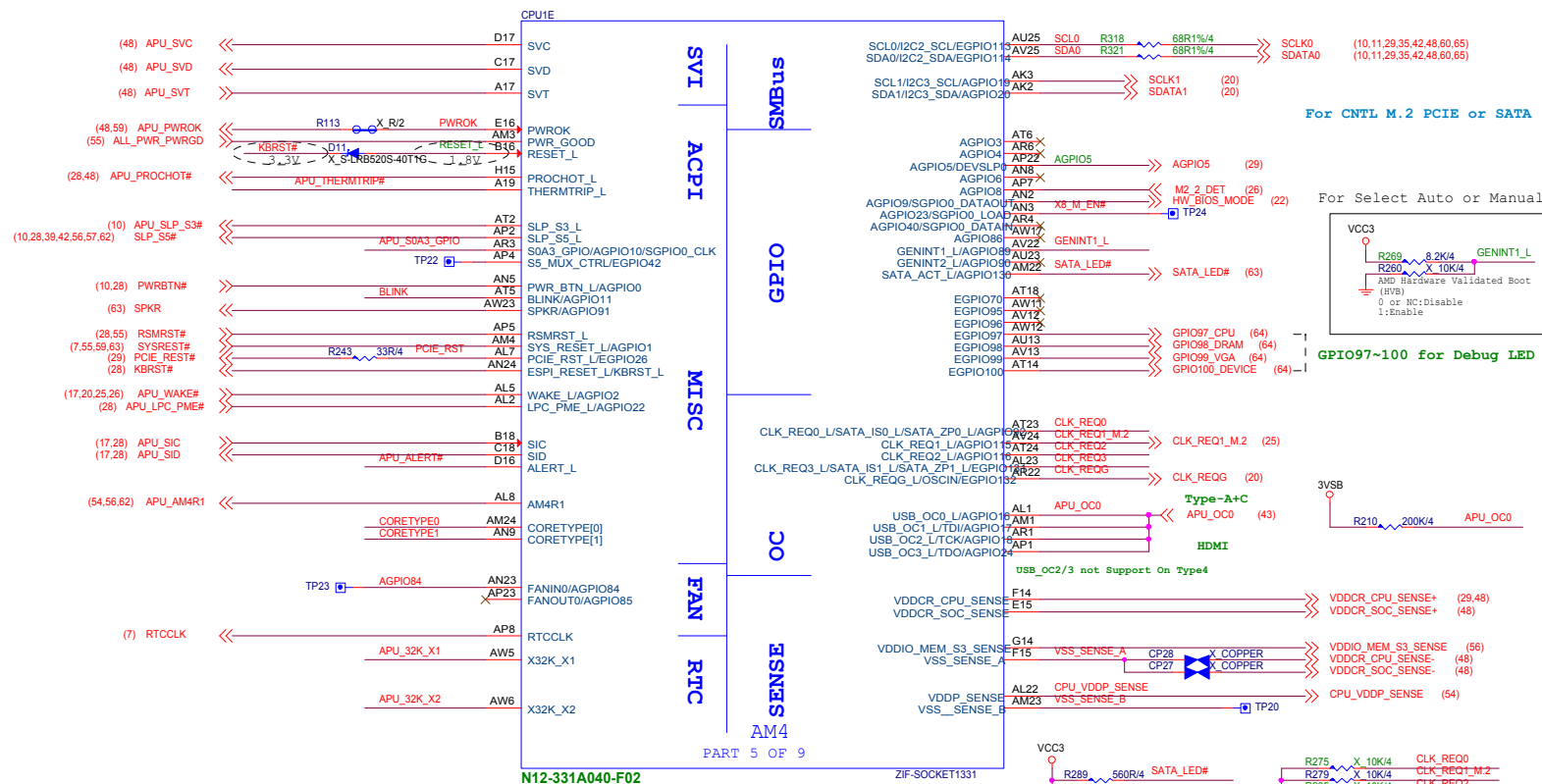
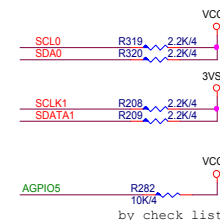
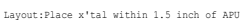
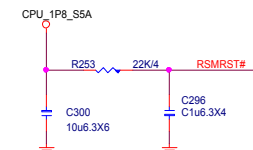
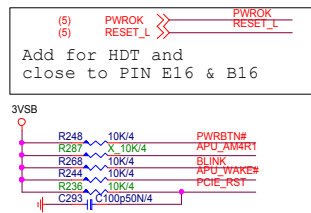
TYPE 0/1	PCIE	SATA
TYPE 2/3/4	2 or 4	2 or 0


PCI_E1 X16
(For Type-2/4)

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15



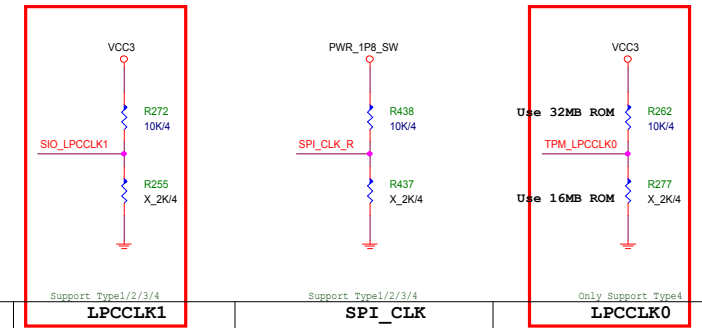


CPU	TYPE	CORETYPE 1	0
SR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1

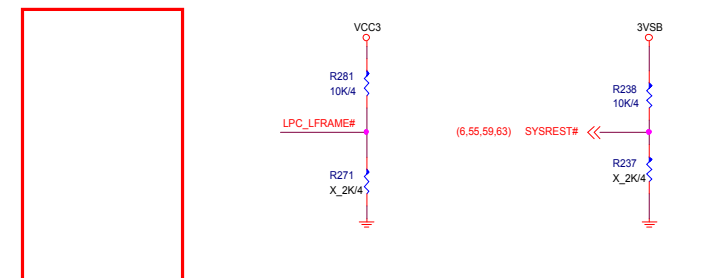


MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description AM4 SV1 / ACPI / GPIO	Rev 1.	
Date: Wednesday, September 25, 2019	Sheet	6	of 75

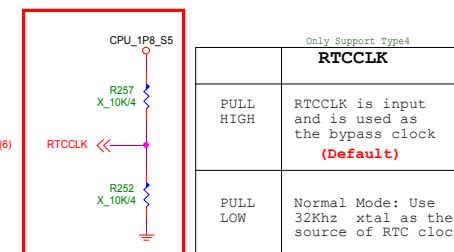
Strapping Options



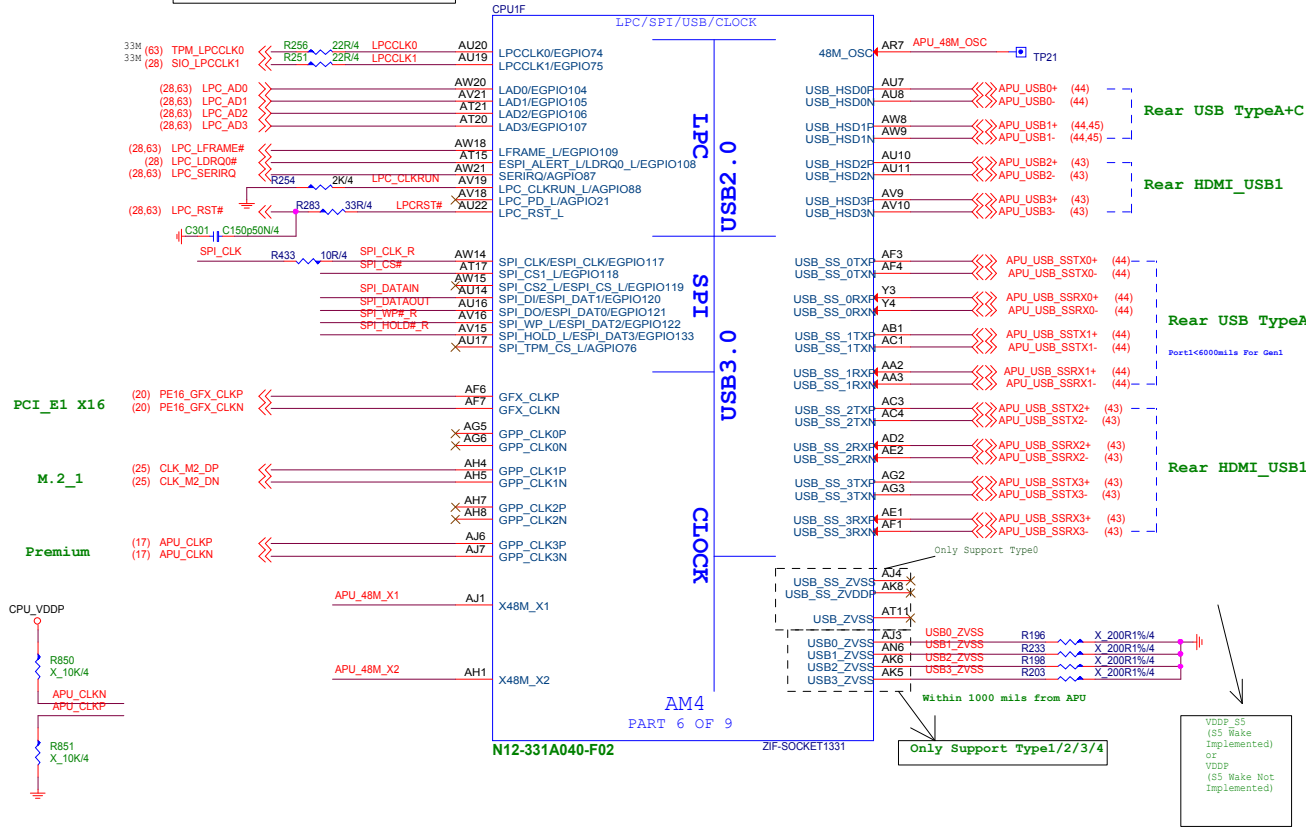
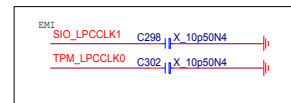
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



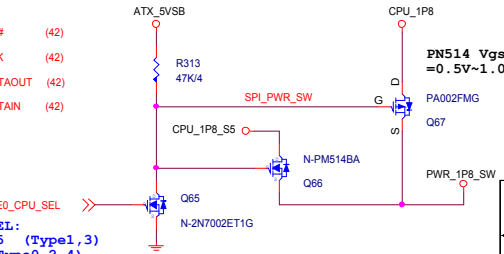
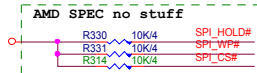
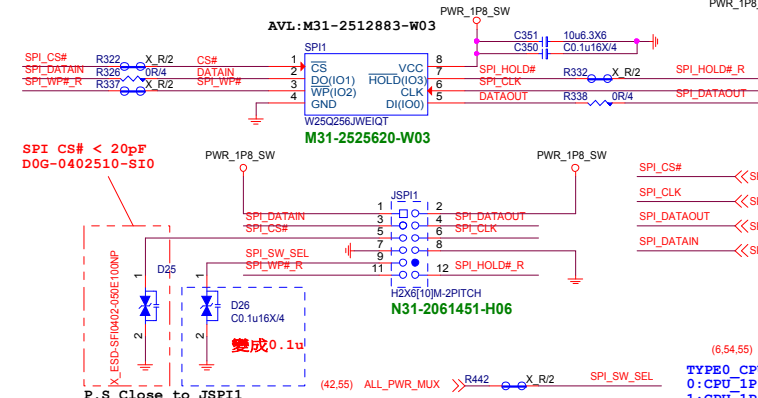
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode



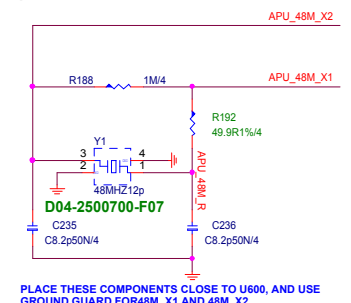
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	AM4 LPC / SPI / USB / CLK / STRAP	1.4
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SPI ROM(1.8V)



Layout:Place x'tal within 1.5 inch of APU



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

GND

AM4
PART 9 OF 9

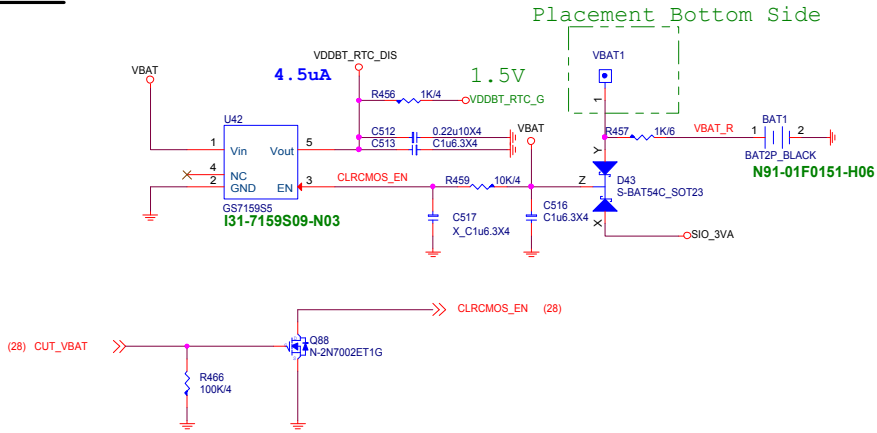


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	AM4 GND	1.4
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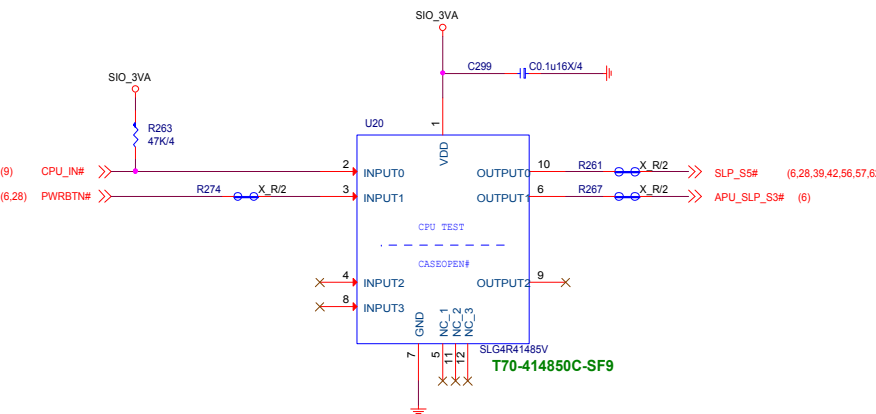
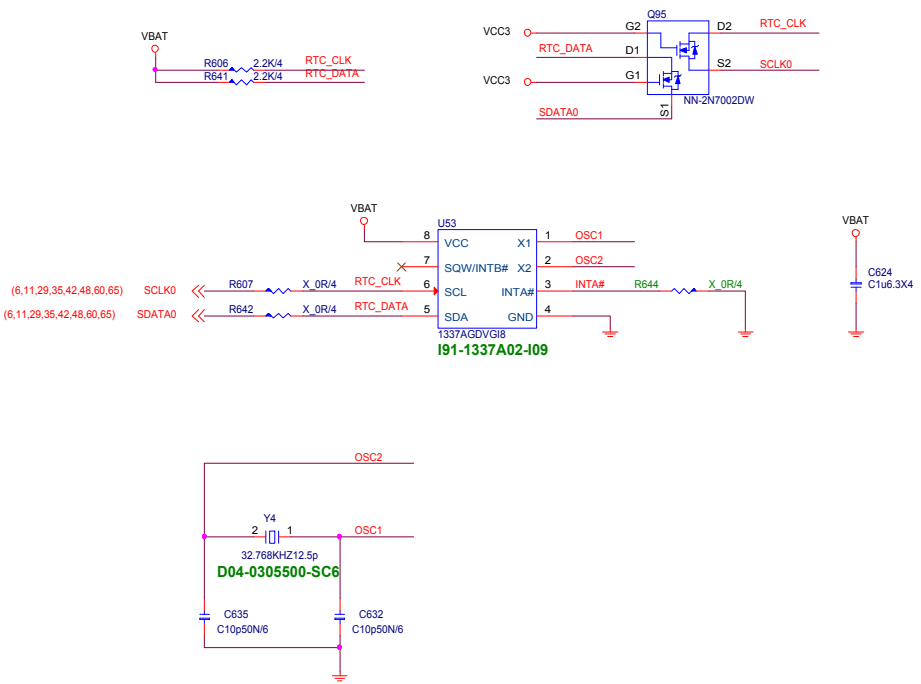
RTC & Clear CMOS Circuit

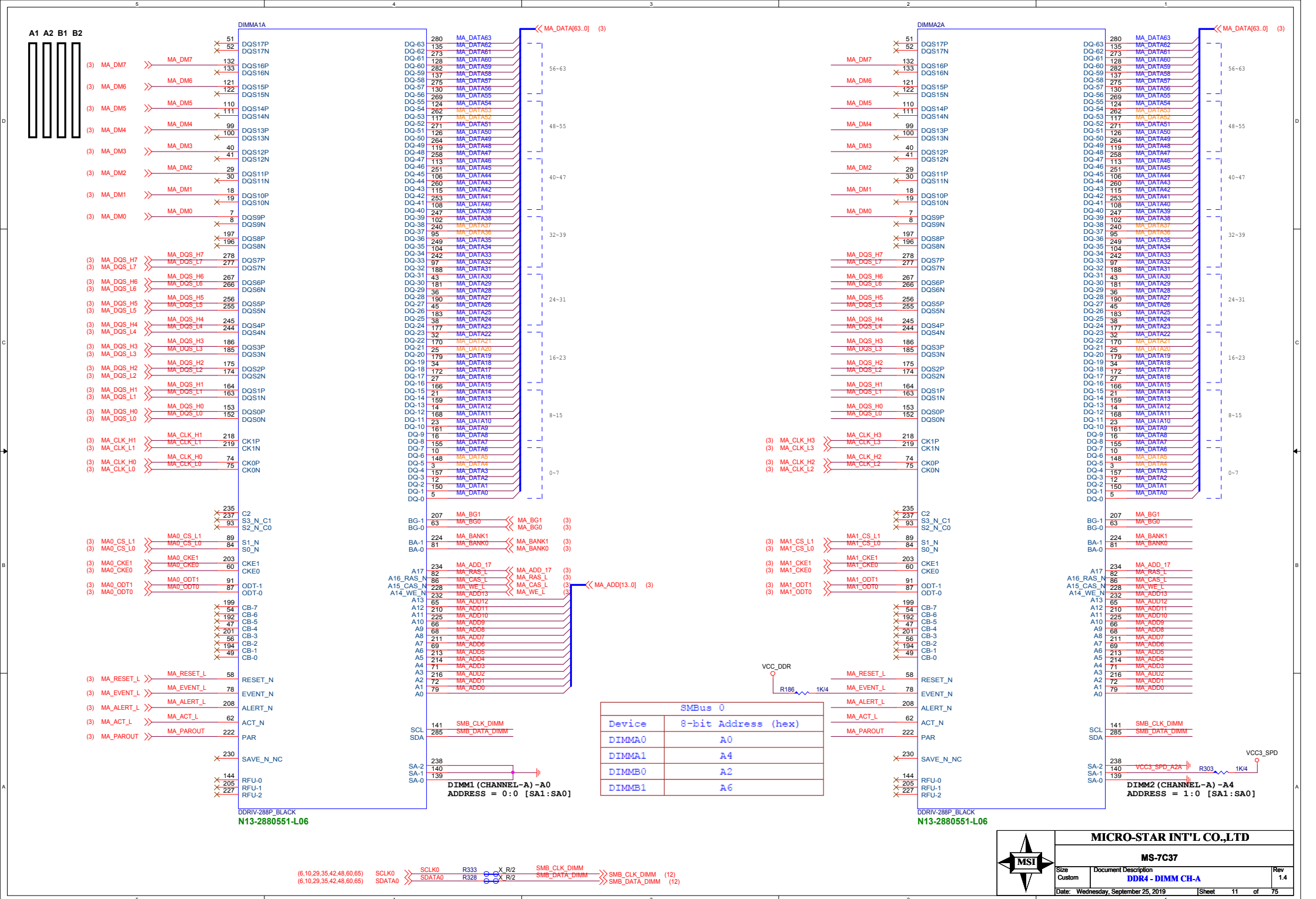


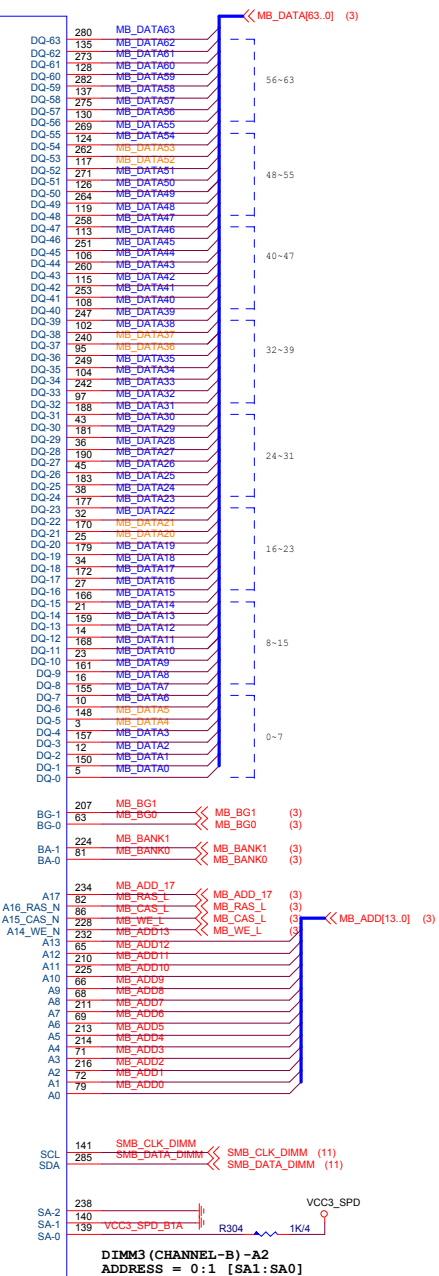
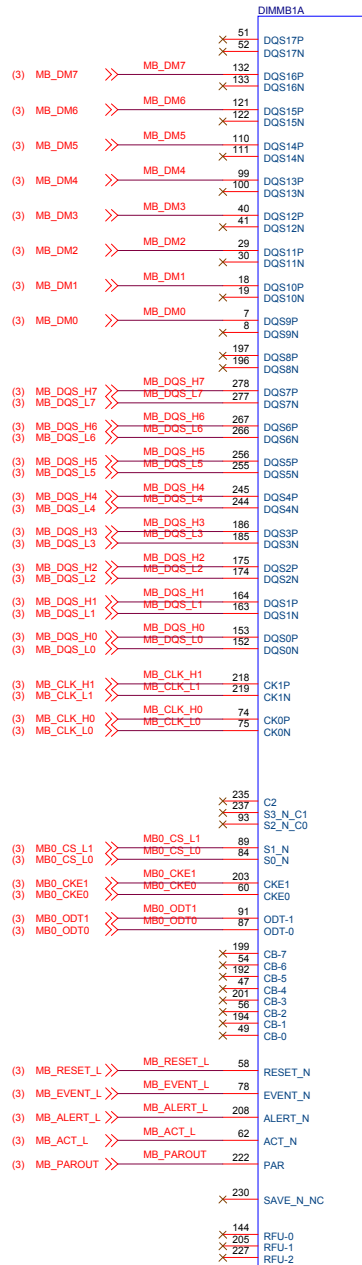
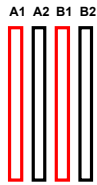
Clear CMOS button



RTC Backup

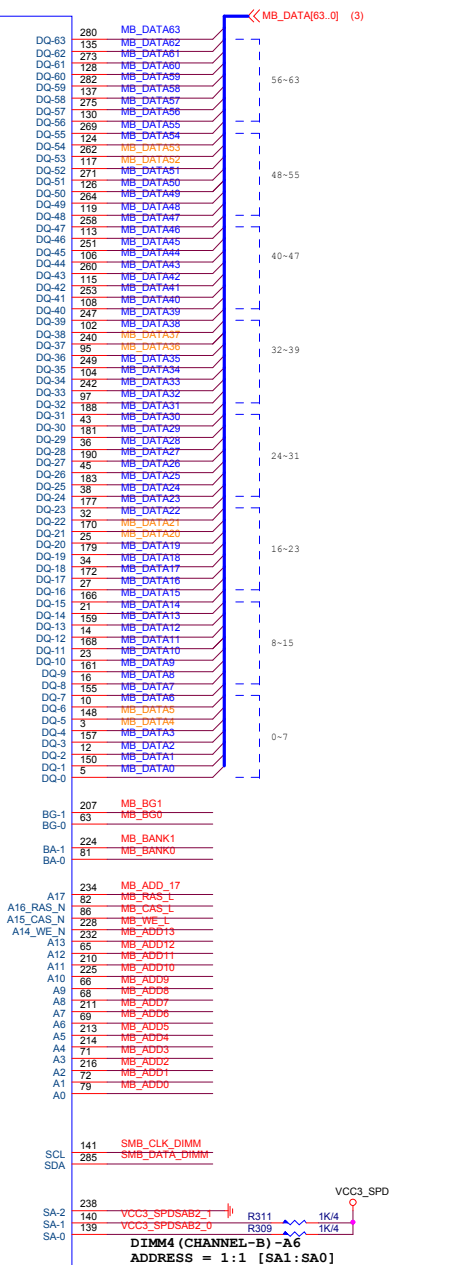
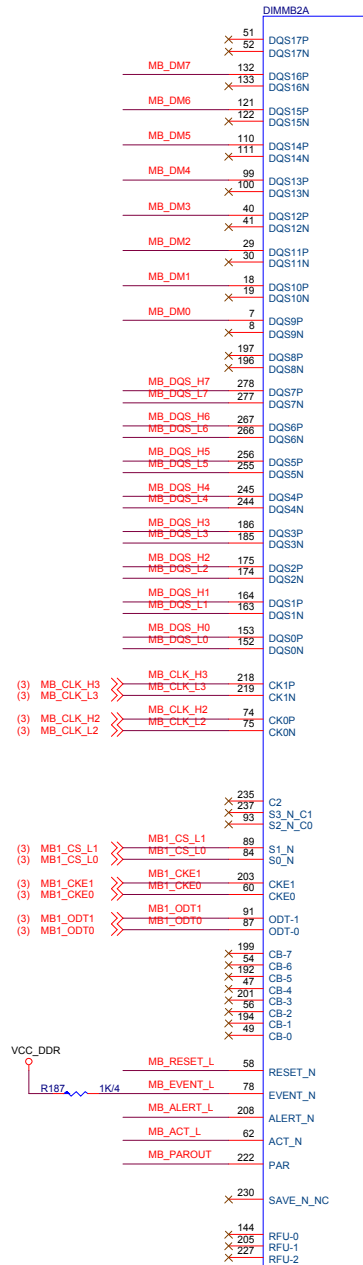






DIMM3 (CHANNEL-B) -A2
ADDRESS = 0:1 [SA1:SA0]

DDRIV-288P_BLACK
N13-2880551-L06



DIMM4 (CHANNEL-B) -A6
ADDRESS = 1:1 [SA1:SA0]

DDRIV-288P_BLACK
N13-2880551-L06

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MS-7C37

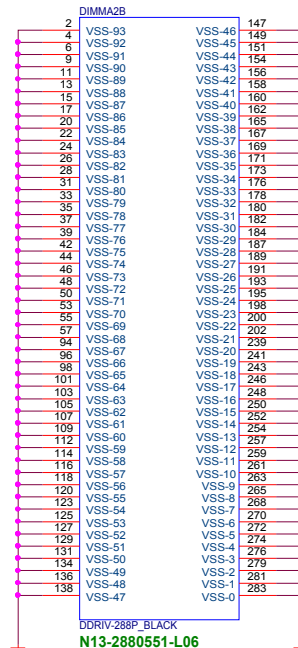
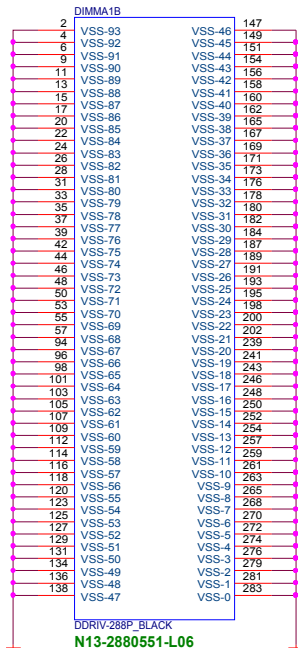
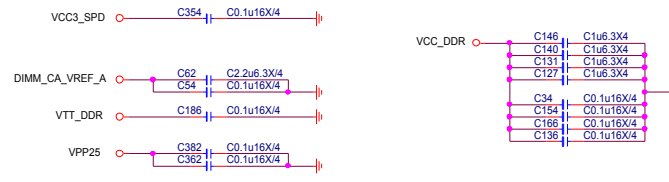
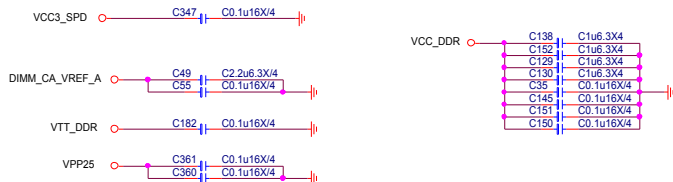
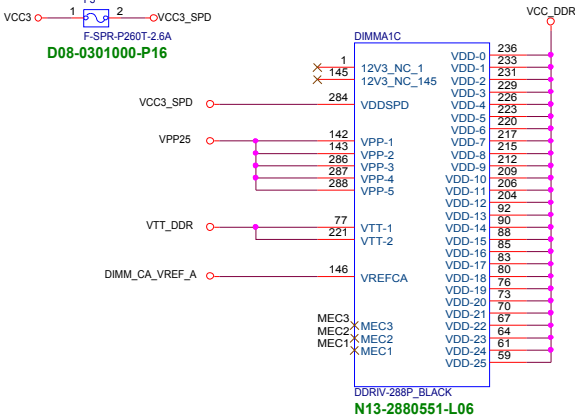
Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	1.4
Date: Wednesday, September 25, 2019		Sheet 12 of 75

av1:D08-0301100-B07

VCC3 SPD
F5
F-SPR-P280T-2.6A

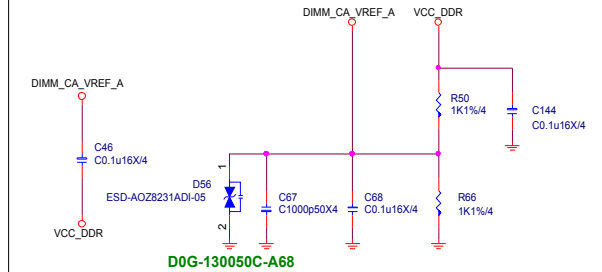
D08-0301000-P16

DIMM SLOT PN BY SPEC



DDR VREF

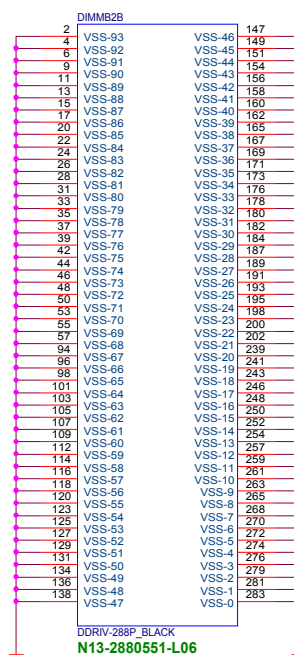
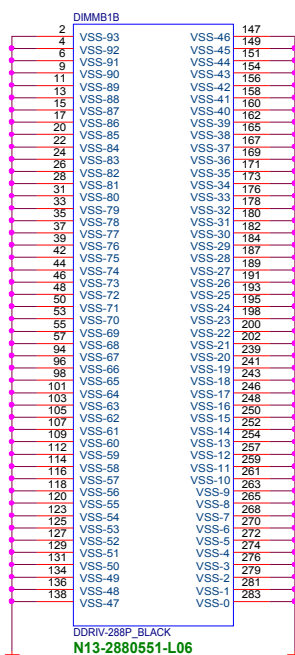
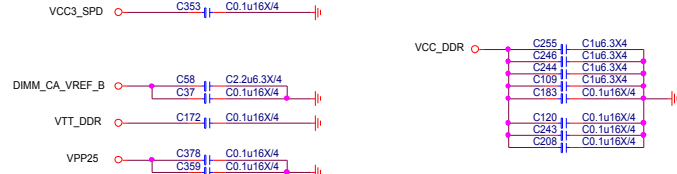
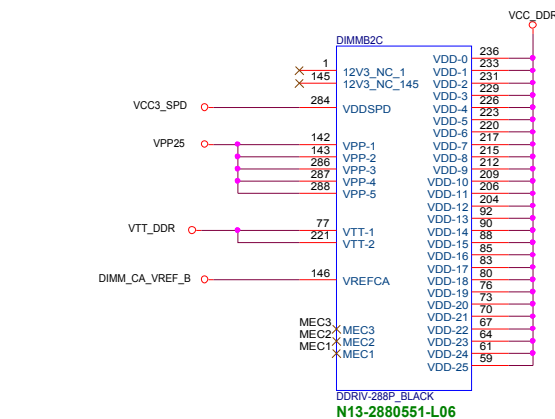
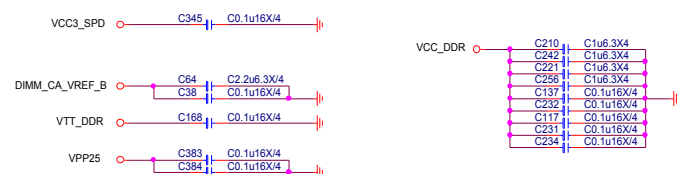
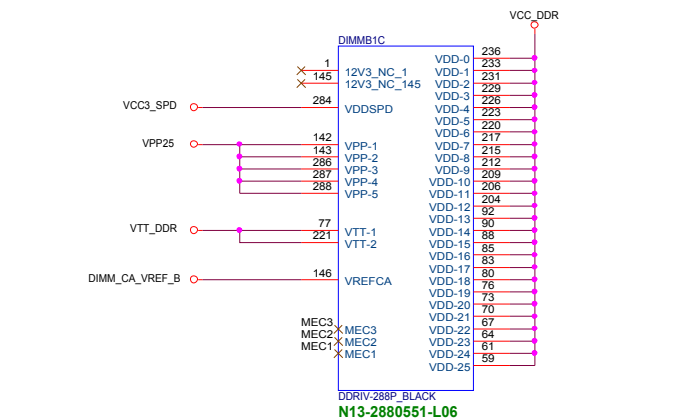
(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD

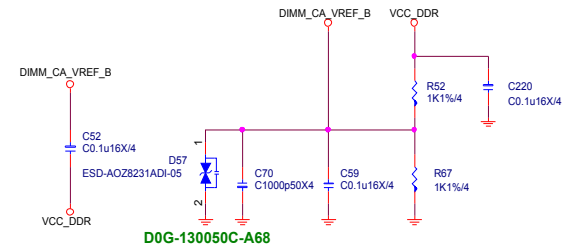
MS-7C37

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	1.4
Date:	Wednesday, September 25, 2019	Sheet 13 of 75



DDR VREF

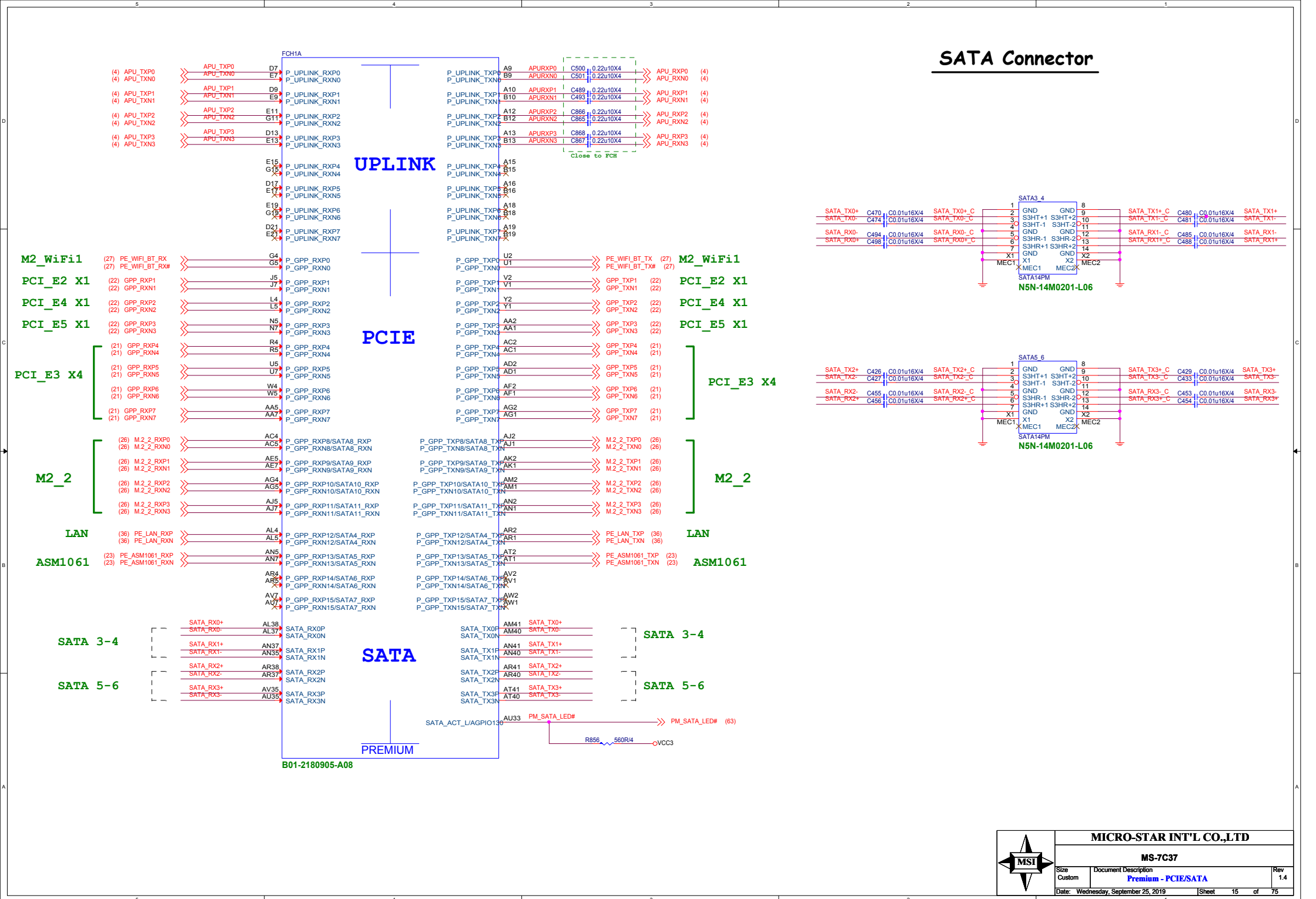
(place resistors close to DIMMs)

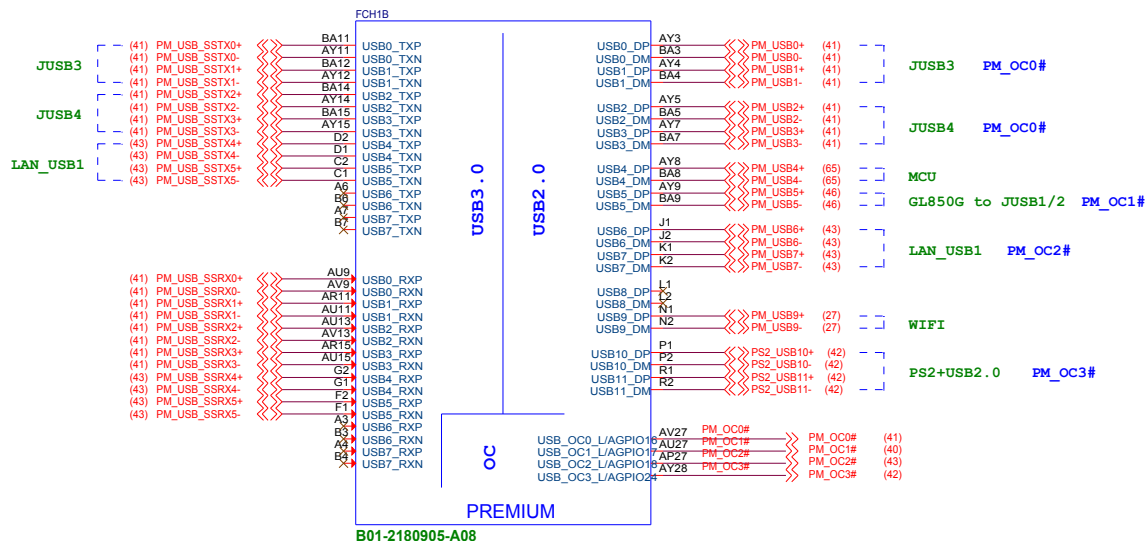


MICRO-STAR INT'L CO.,LTD

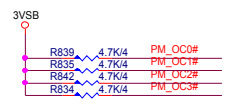
MS-7C37

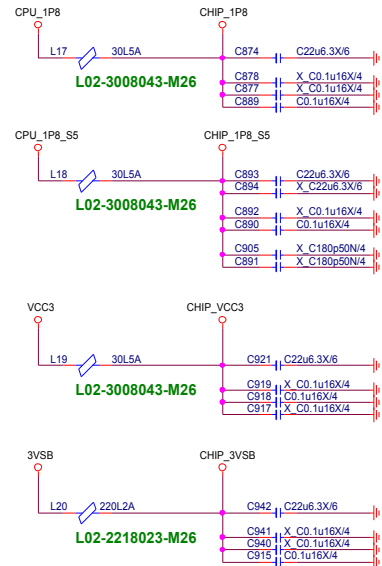
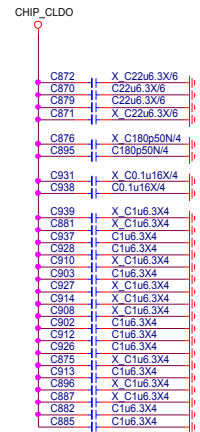
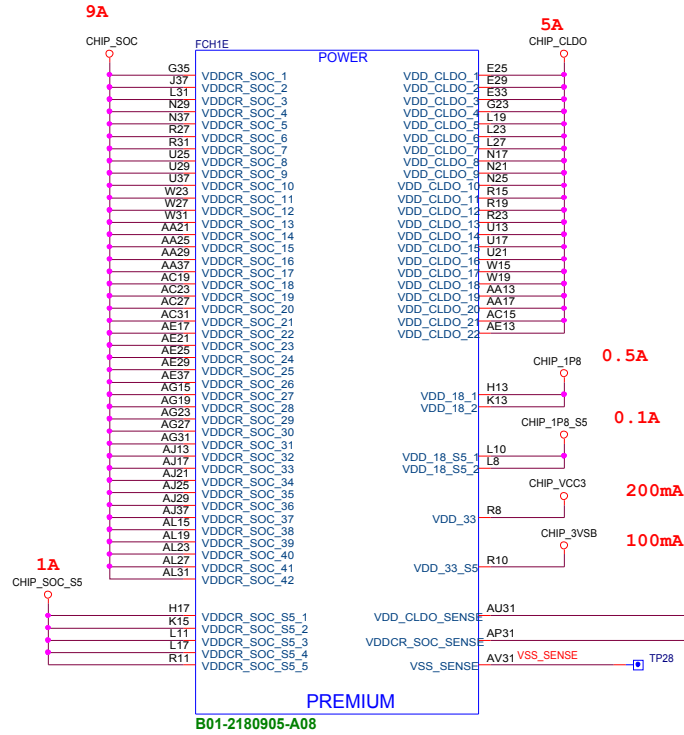
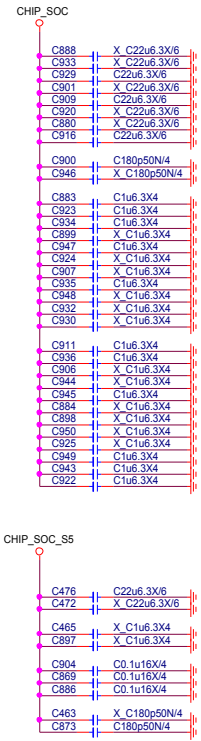
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	1.4
Date: Wednesday, September 25, 2019	Sheet 14 of 75	

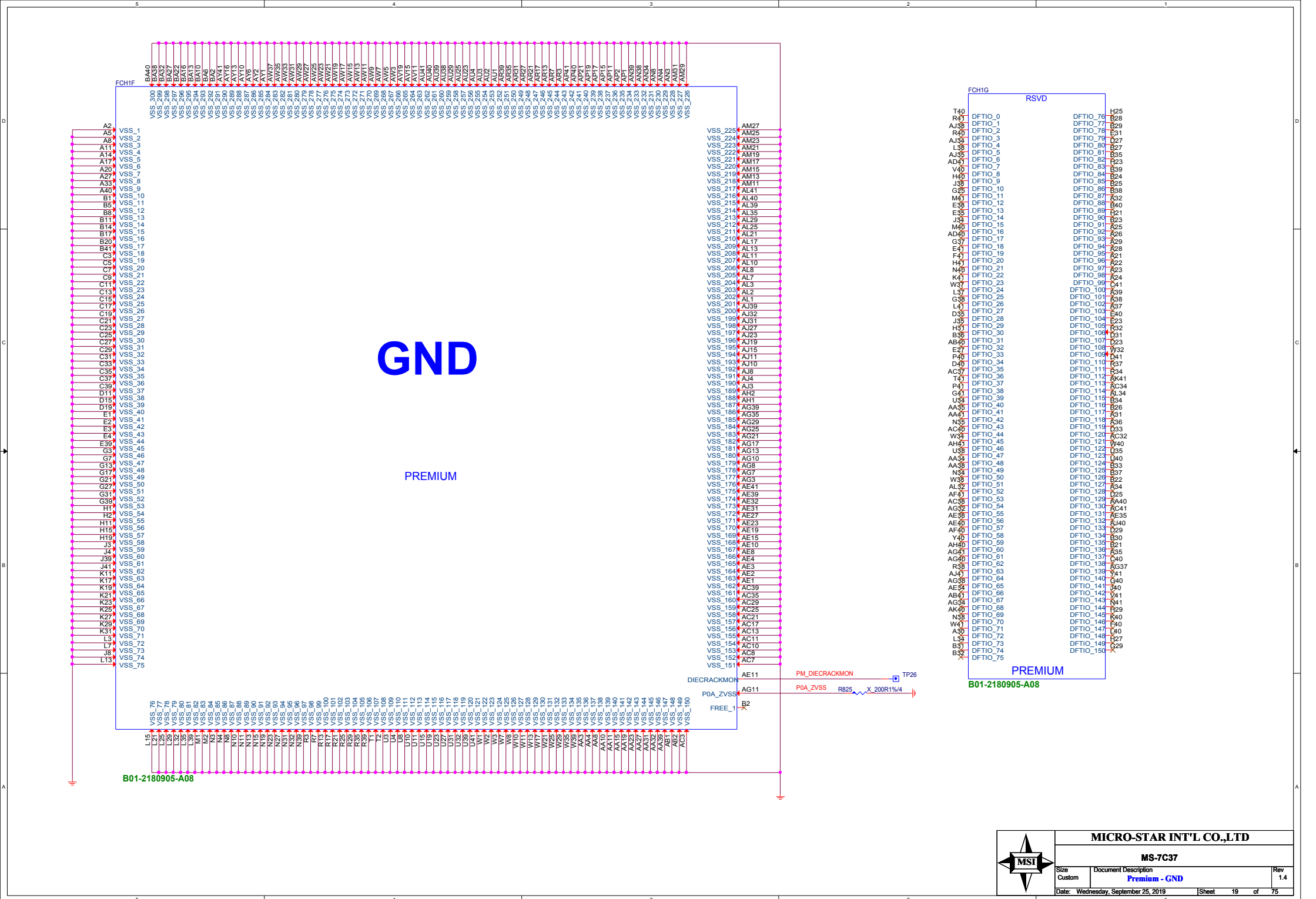




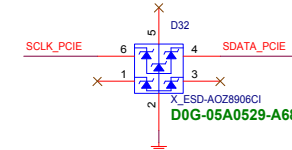
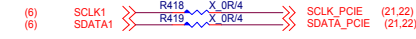
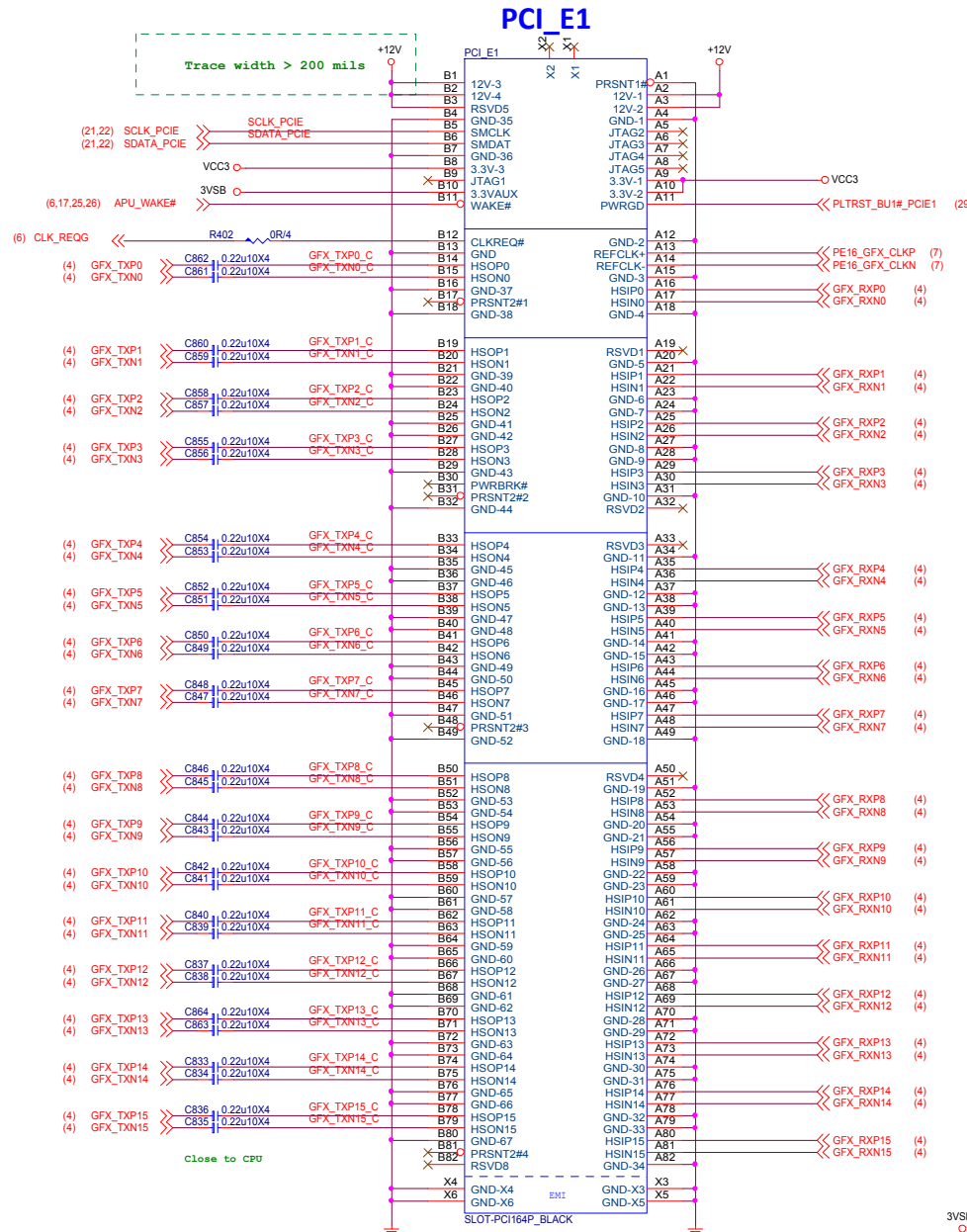
Ports	Host Controller	OC Pin
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC1



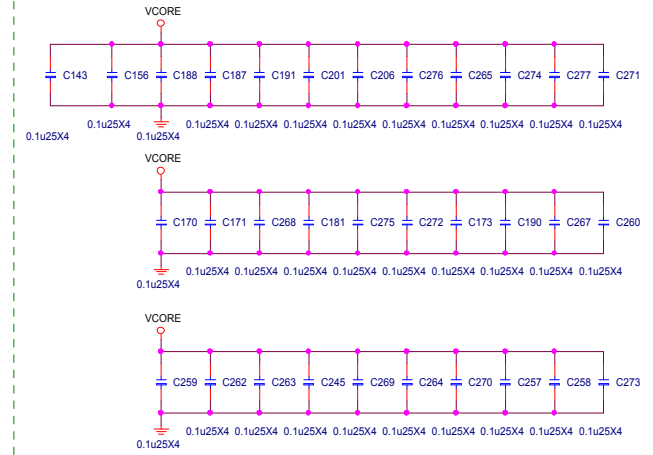




PCI EXPRESS x16 Slot



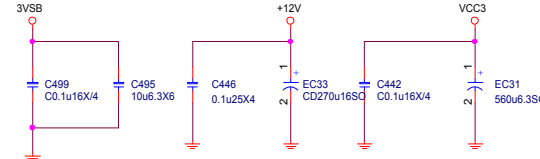
Bypass Capacitor For Across Moat



PCI Express x16 Slot

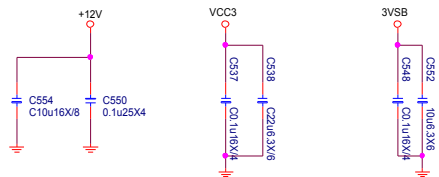
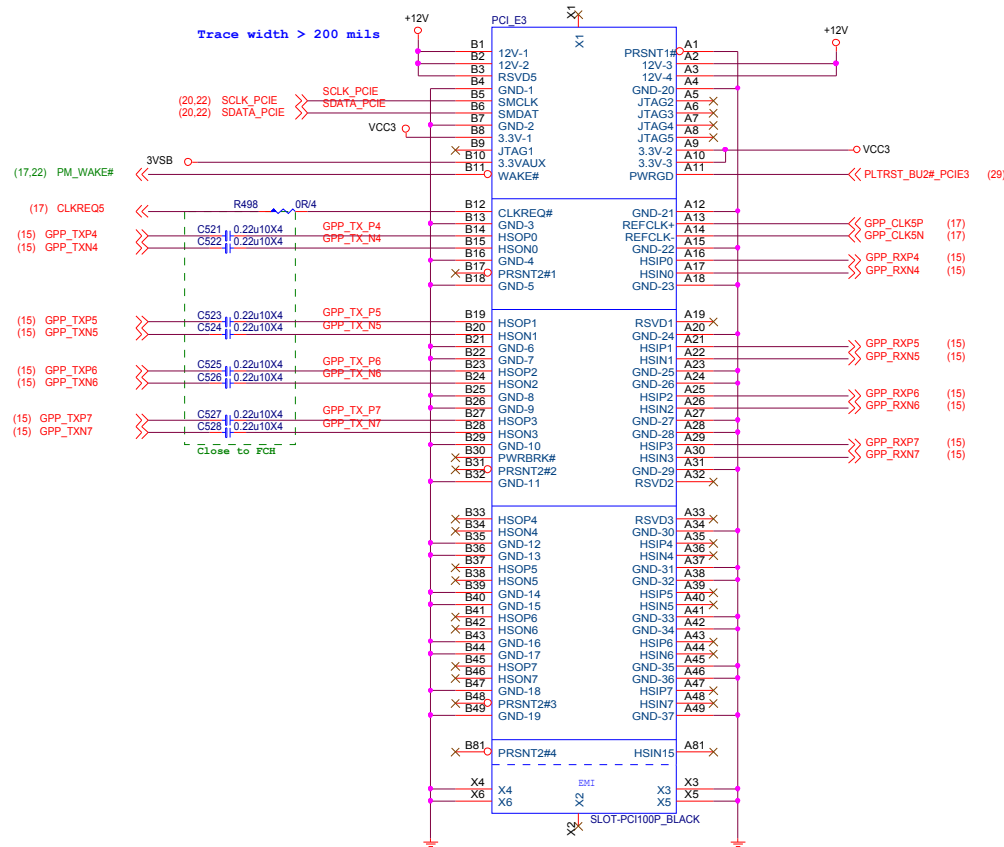
+12V	- 5.5A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA

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MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 1.4
PCI E1 (X16)		
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PCI_E3 X4



PCI Express x4 Slot *1

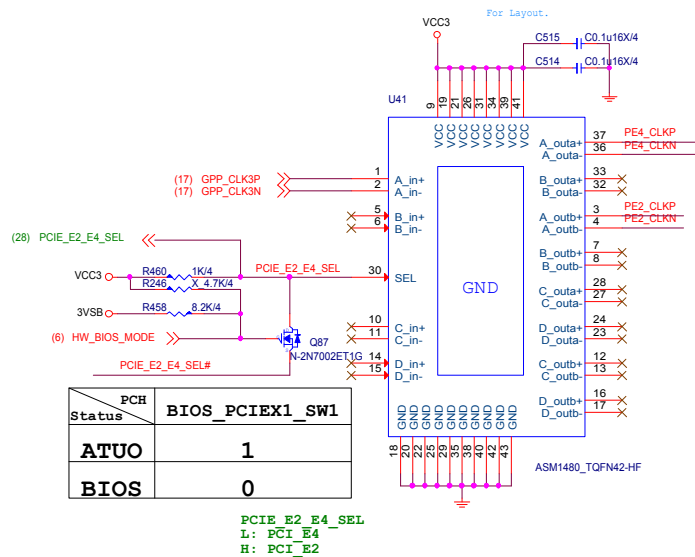
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



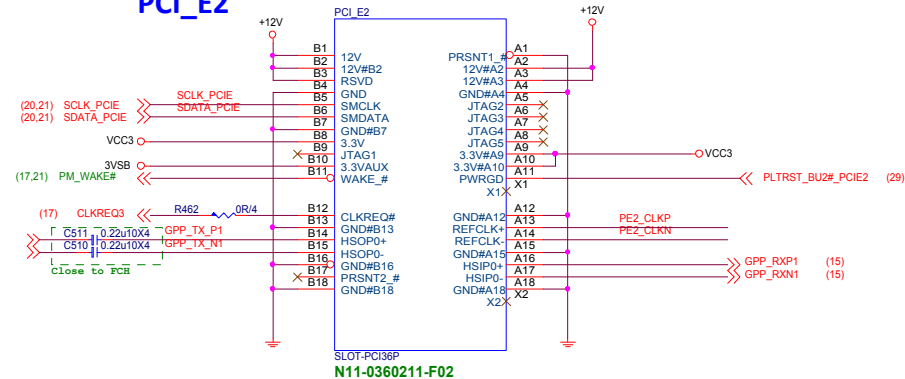
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	PCI_E3 (X4)	1.4
Date: Wednesday, September 25, 2019	Sheet 21 of 75	

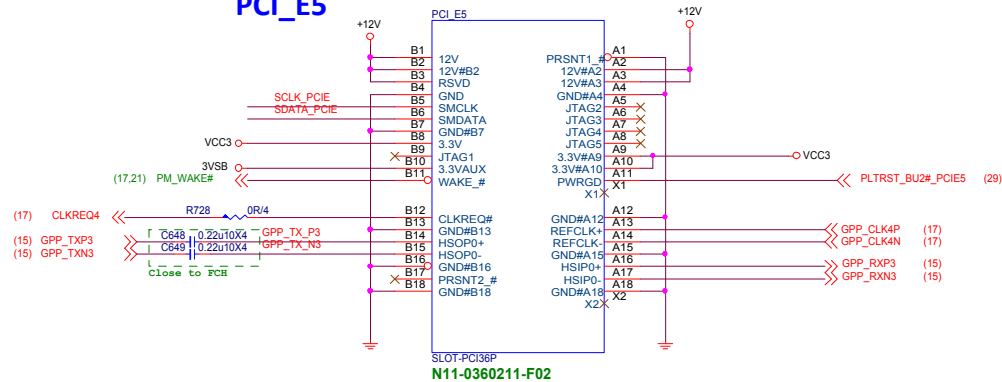


PCI_E2

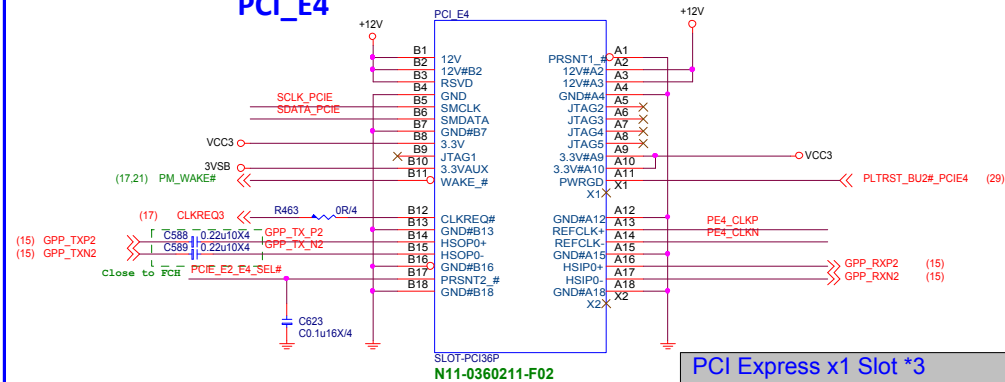


PCIE_E2 & PCIE_E4互切, PCIE_E2 & PCIE_E4同时有PCIE device 以PCIE_E4 优先

PCI_E5



PCI_E4



PCI Express x1 Slot *3

+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



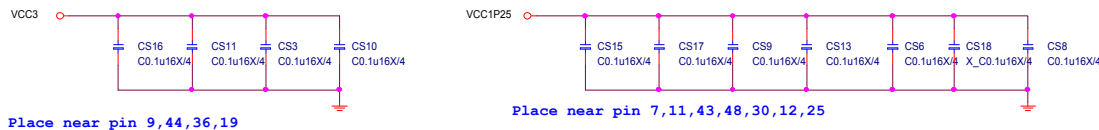
MICRO-STAR INT'L CO.,LTD

MS-7C37

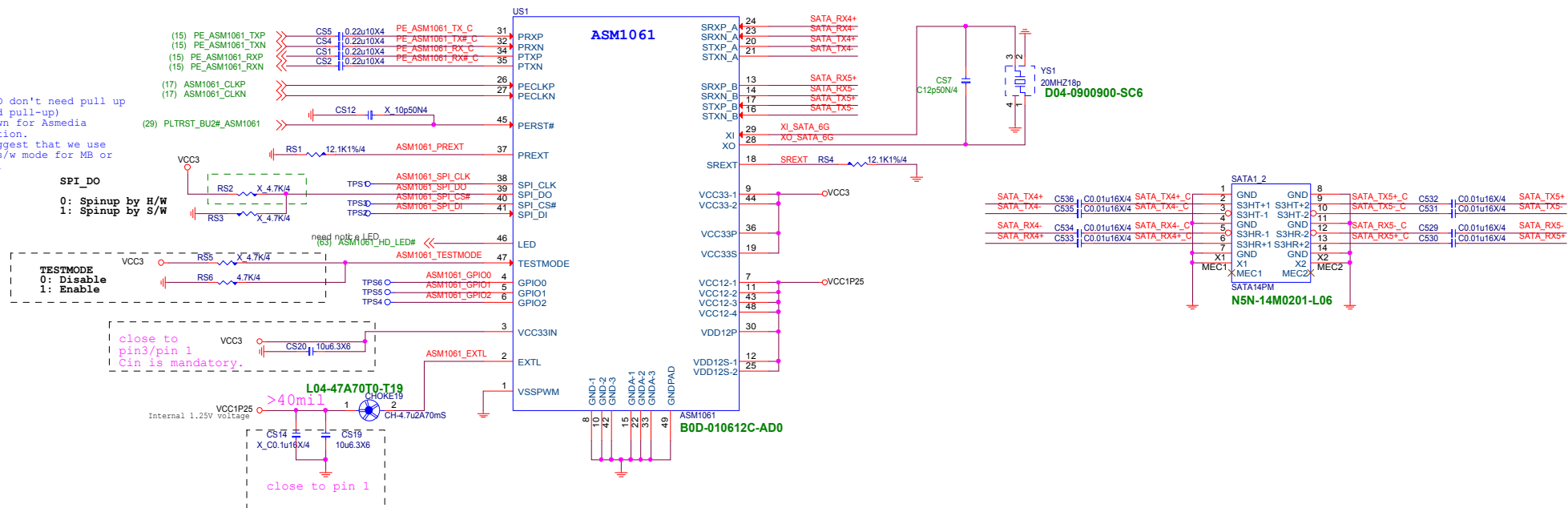
Size	Document Description	Rev
Custom	PCIE Switch PCI_E2 / E4 / E5 (X1)	1.4
Date: Wednesday, September 25, 2019	Sheet 22 of 75	


1.2V delay from 3.3V 90% > 0ms

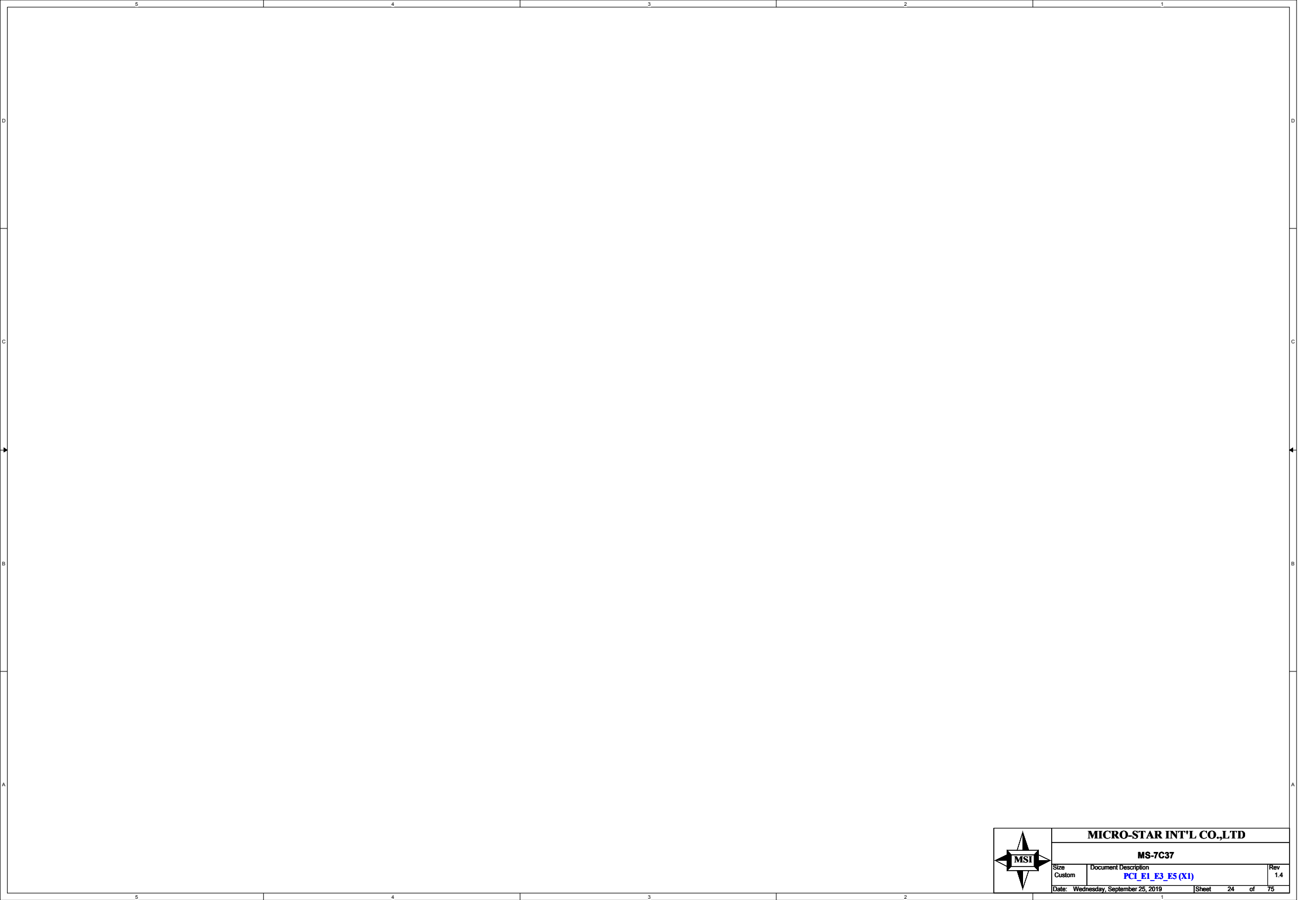
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



SATA SPI DO don't need pull up
(integrated pull-up)
or pull down for Asmedia
recommendation.
Asmedia suggest that we use
spinup by s/w mode for MB or
PCI-E Card.

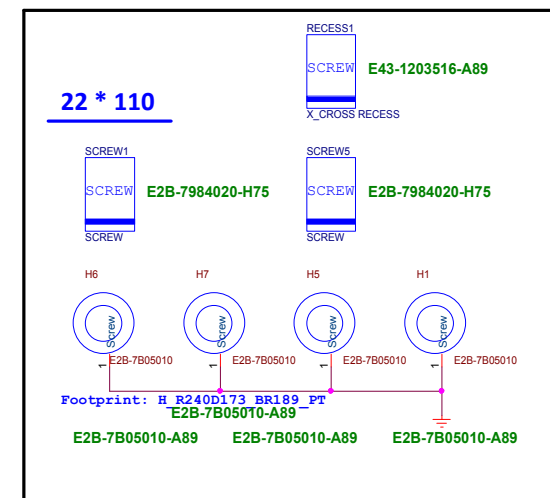
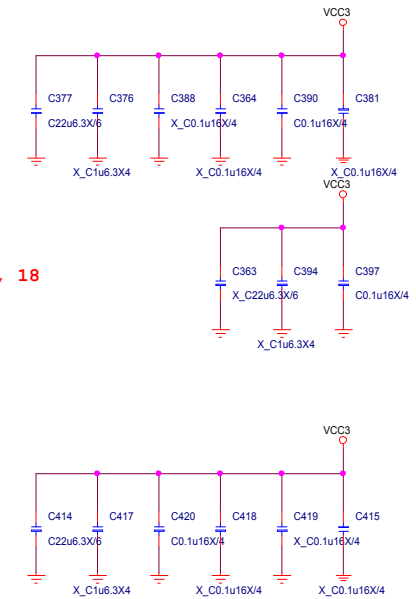


	MICRO-STAR INT'L CO.,LTD		
	MS-7C37		
	Size Custom	Document Description PCIE to SATA (ASMI061)	Rev 1.4
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MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description PCL E1_E3_E5 (X1)	Rev 1.4
Date: Wednesday, September 25, 2019	Sheet 24 of 75	1

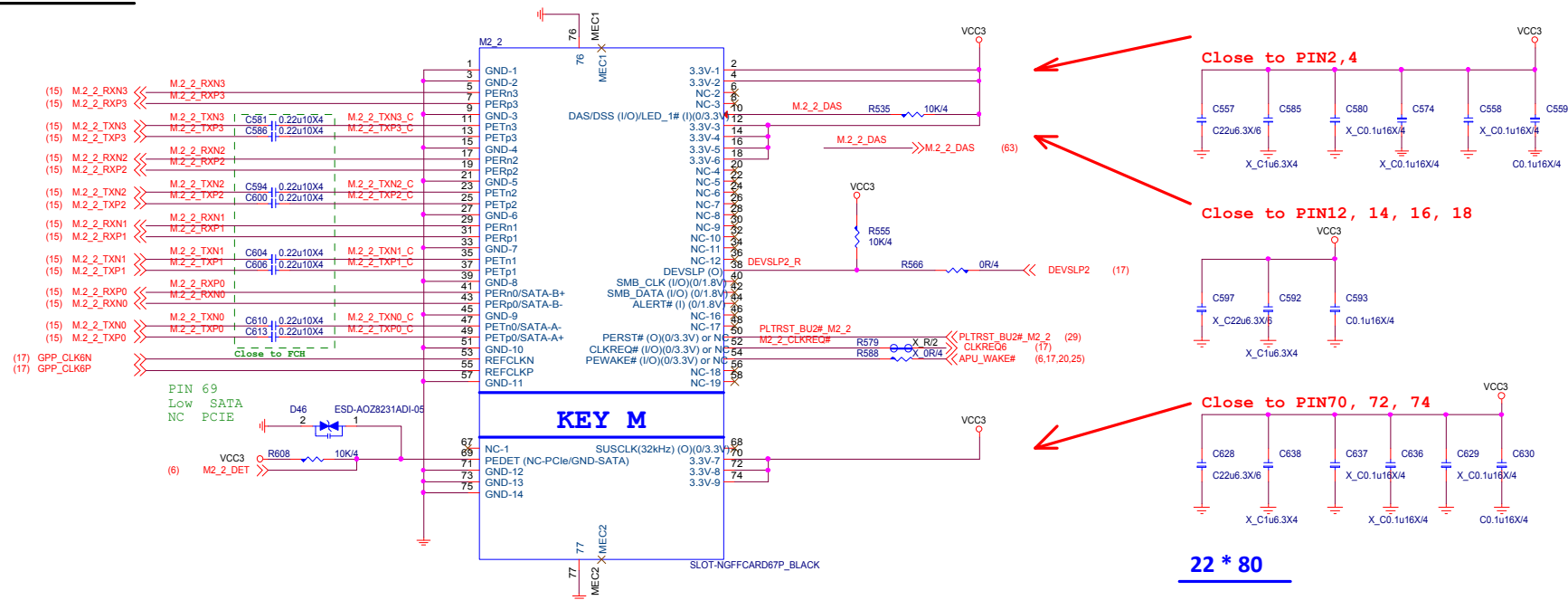
VCC3 4.25A
Max: 14W



MS-7C37

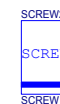
Size	Document Description	Rev
Custom	M2_1	1.4
Date: Wednesday, September 25, 2019		Sheet 25 of 75

M.2_2 Connector

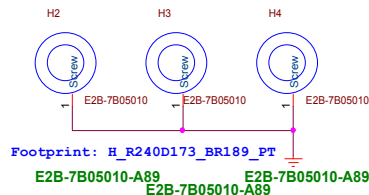


Support PCIE and SATA Mode

22 * 80



E2B-7984020-H75



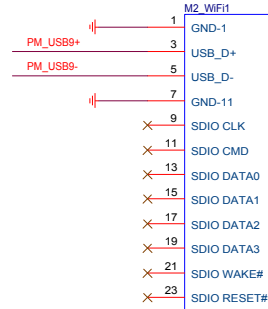
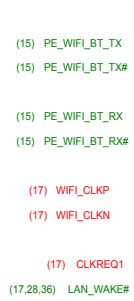
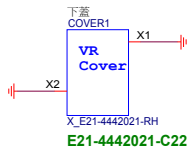
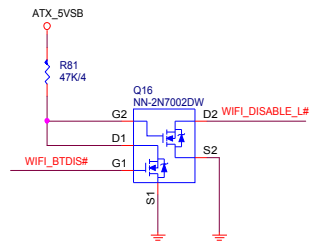
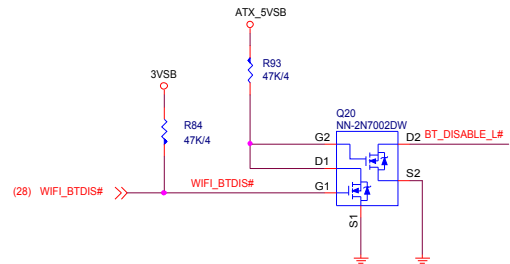
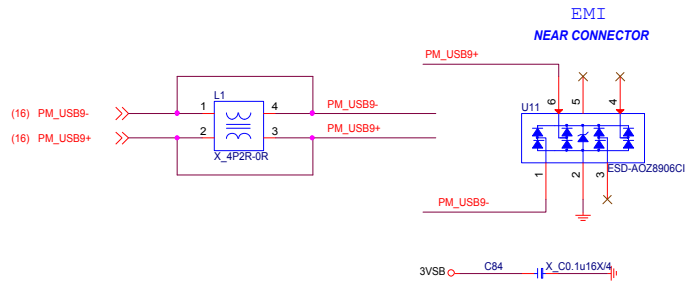
Vinafix.com



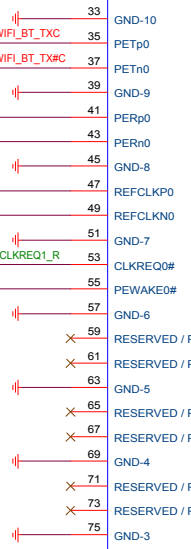
MICRO-STAR INT'L CO.,LTD

MS-7C37

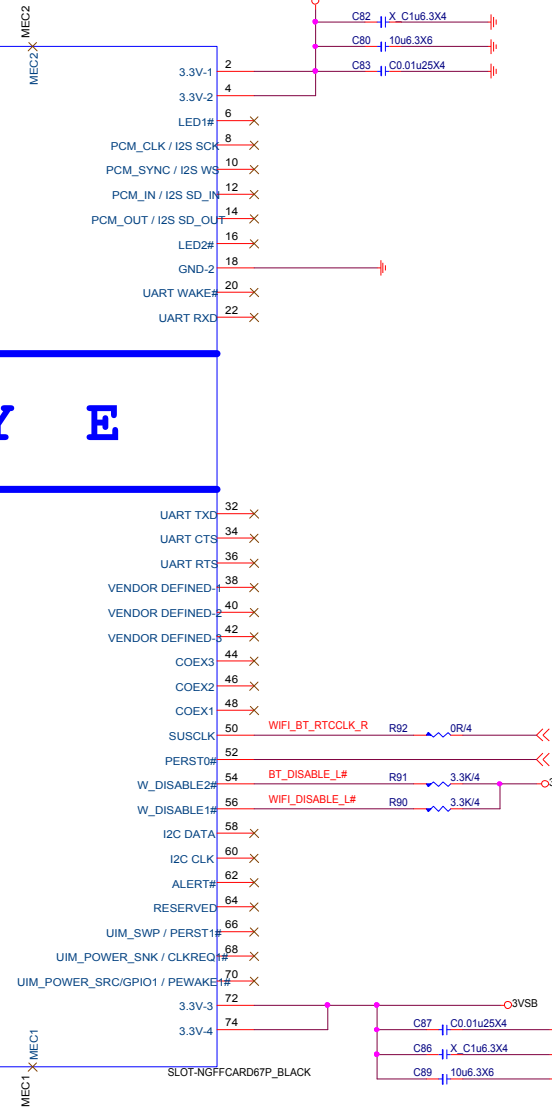
Size	Document Description	Rev
Custom	M2_2	1.4
Date: Wednesday, September 25, 2019		Sheet 26 of 75



KEY E

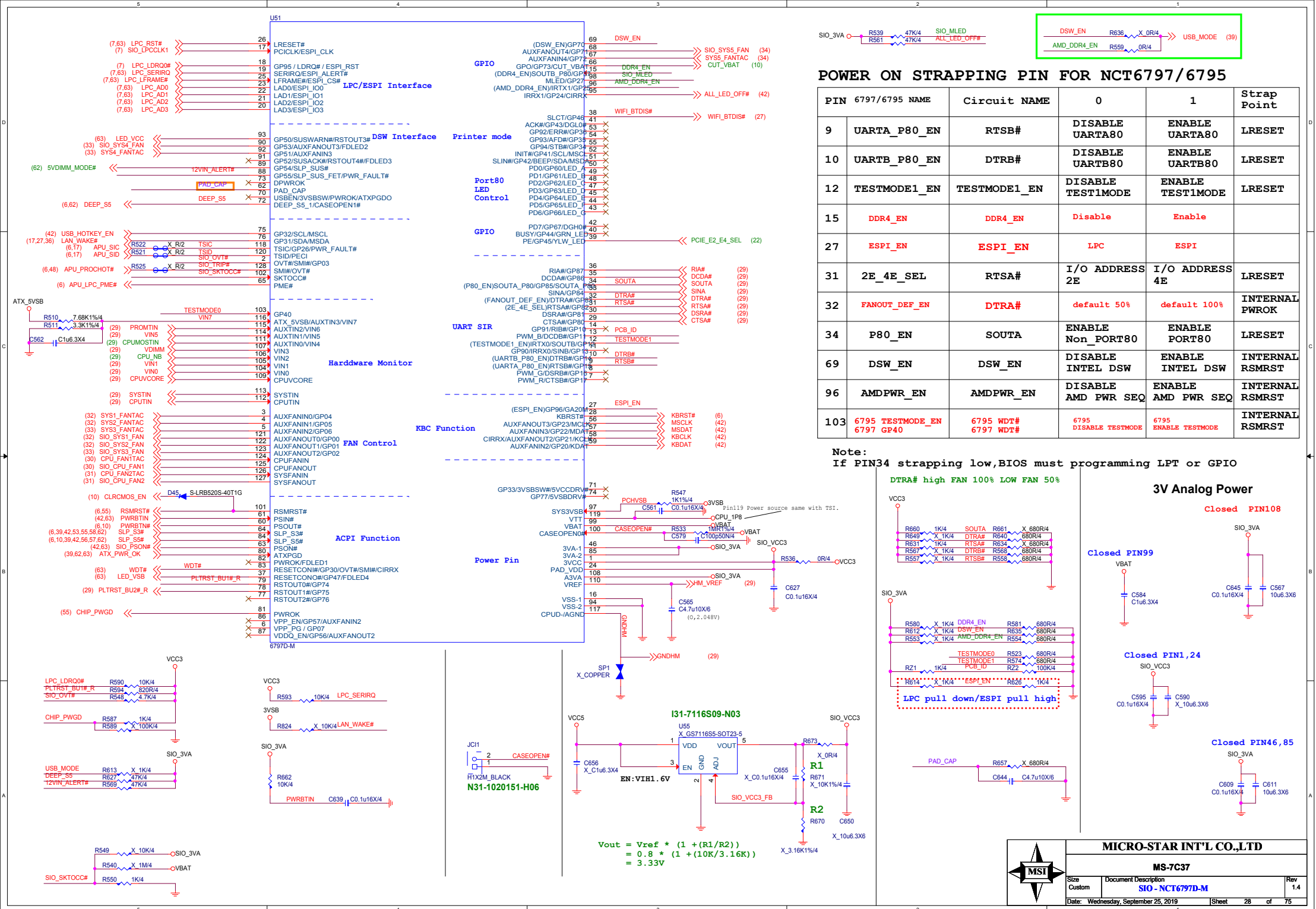


N15-0670610-L06



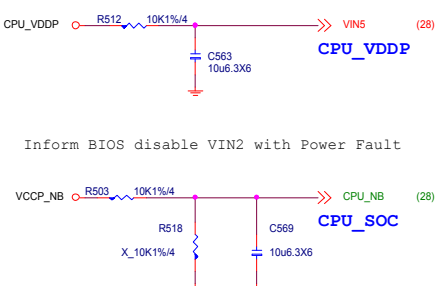
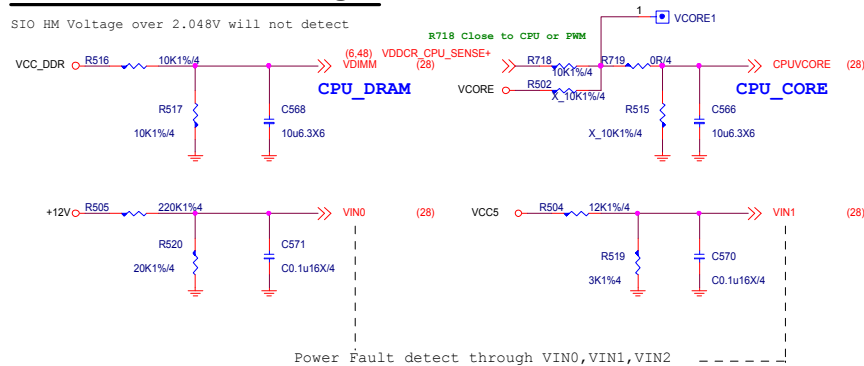
10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.

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MS-7C37			
Size	Document Description		Rev
Custom	M2_WIFI+BT		1.4
Date:	Wednesday, September 25, 2019	Sheet	27 of 75

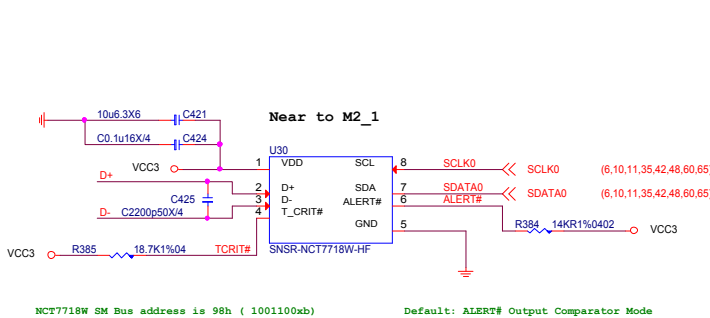


HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



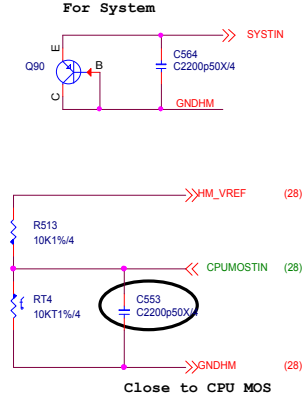
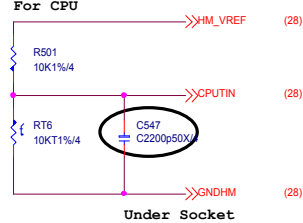
NCT7718W



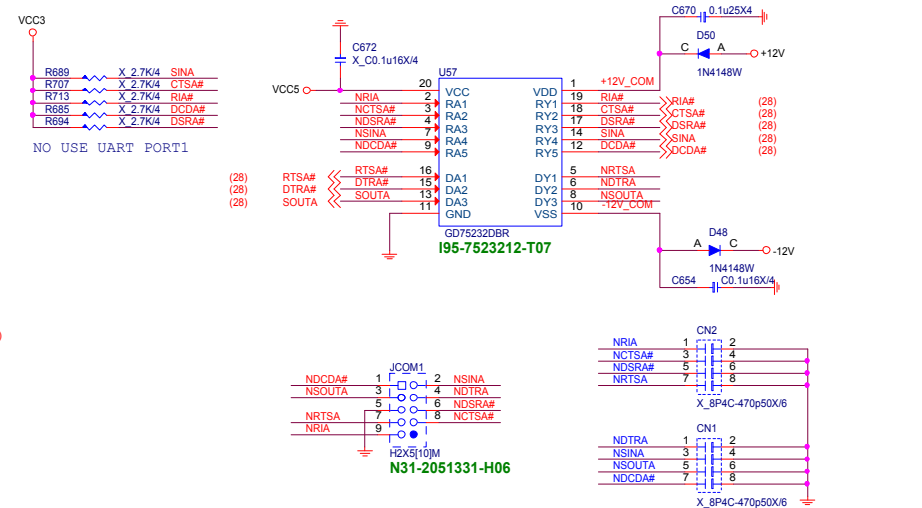
TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115

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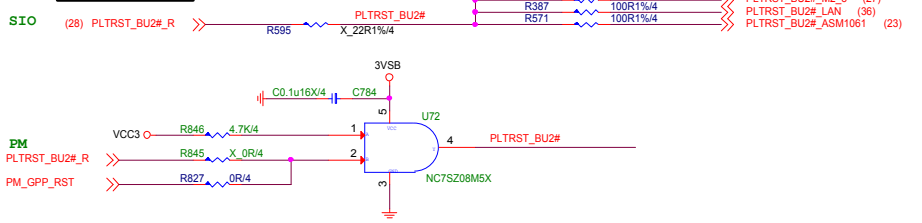
TEMP SENSOR



COM PORT



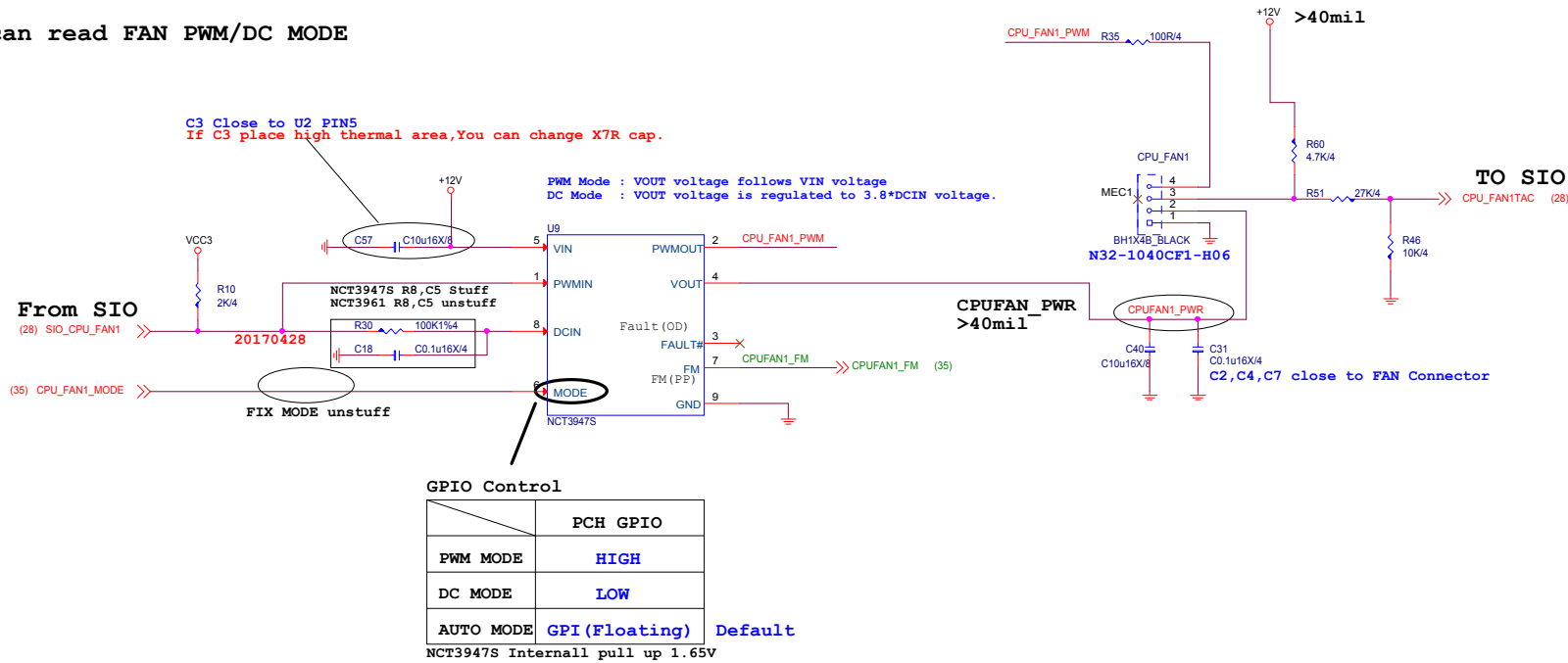
PM RESET



TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

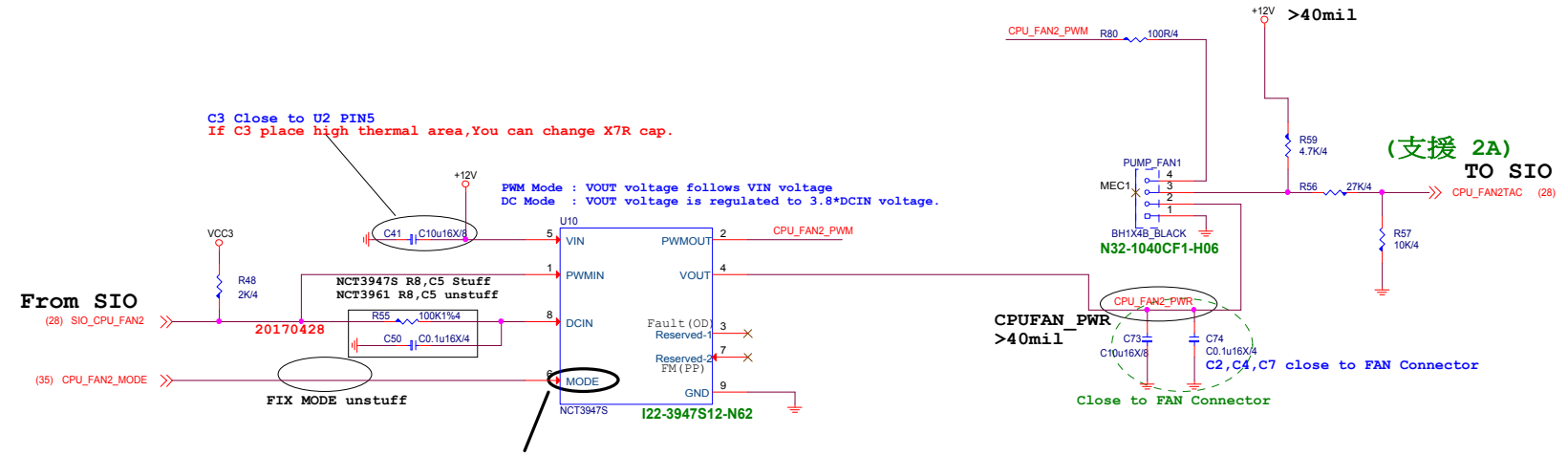
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

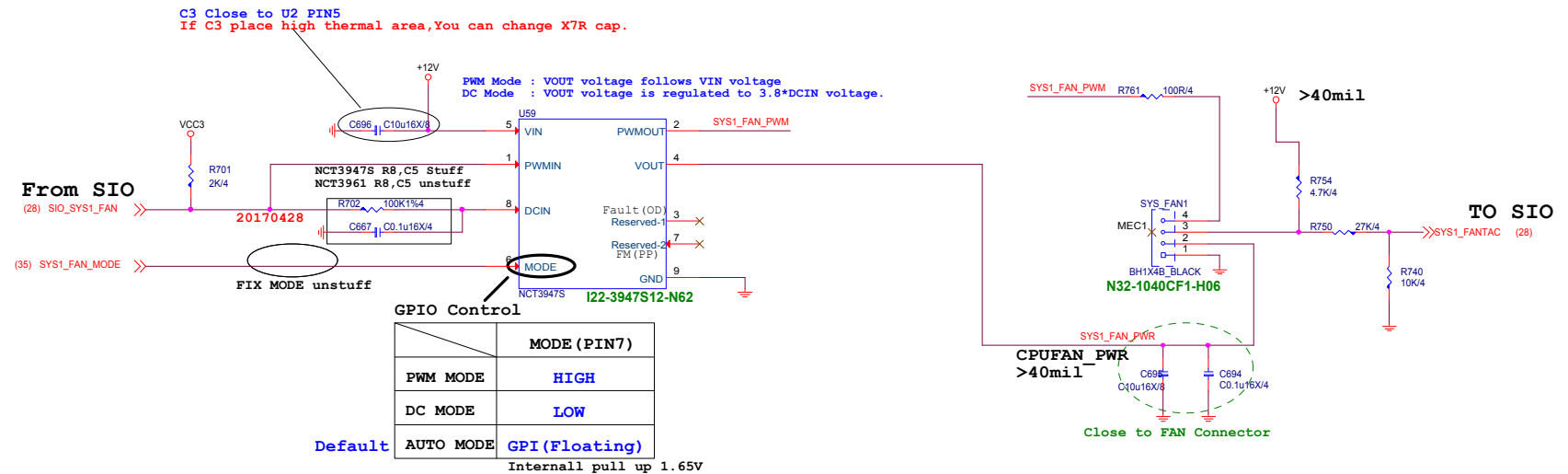
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

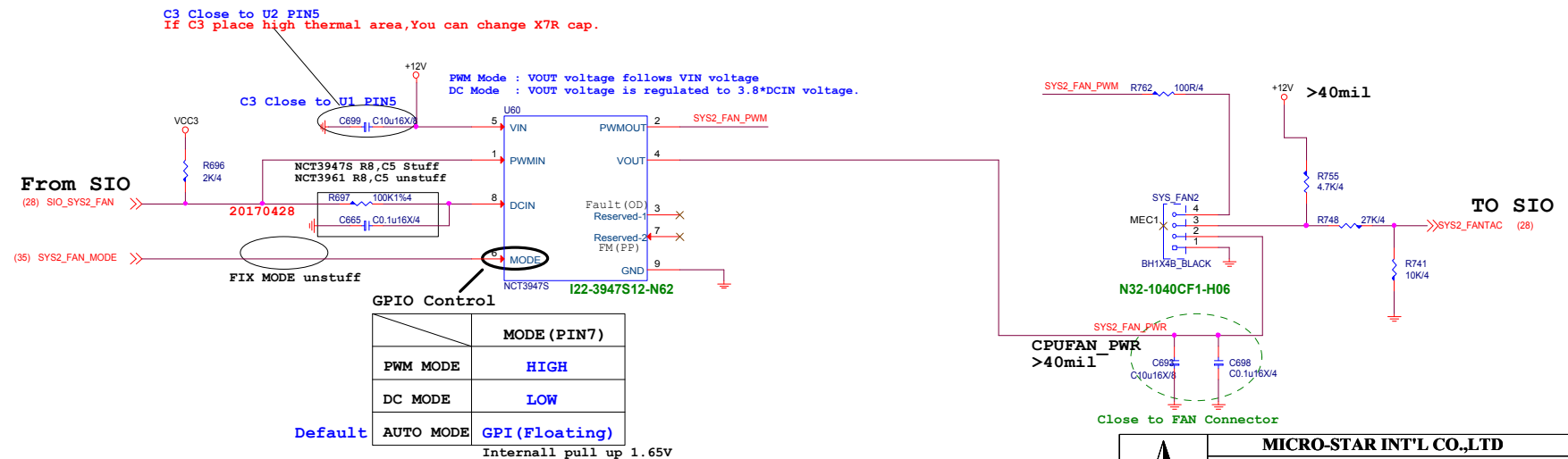
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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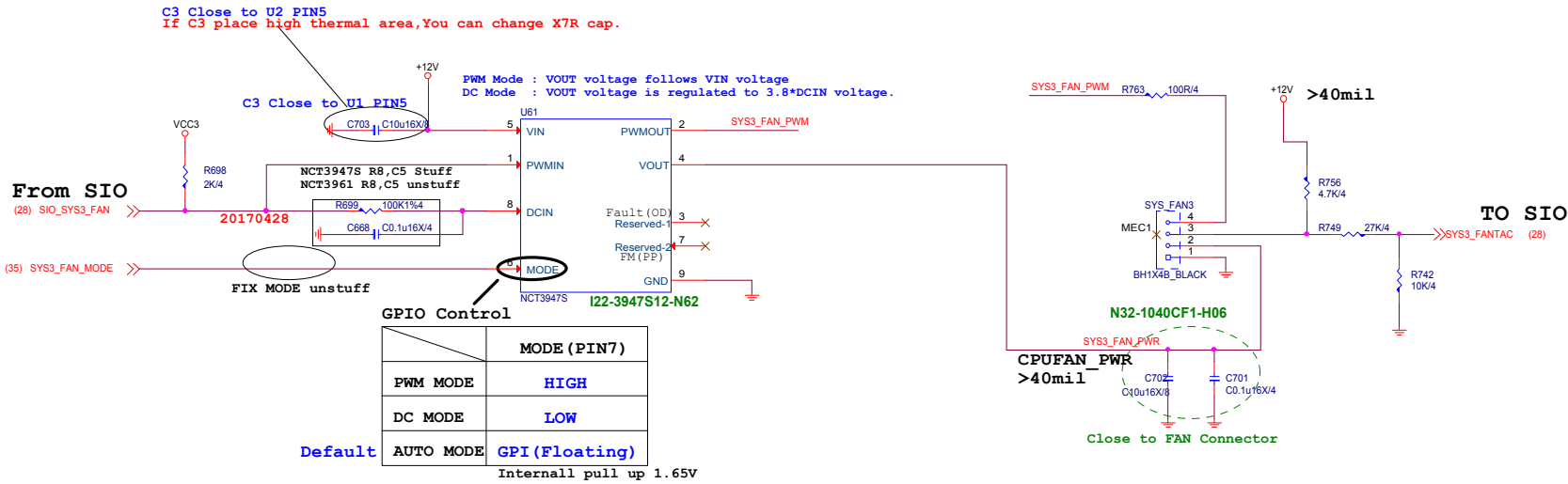
MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	1.4
Date: Wednesday, September 25, 2019	Sheet 32 of 75	

SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

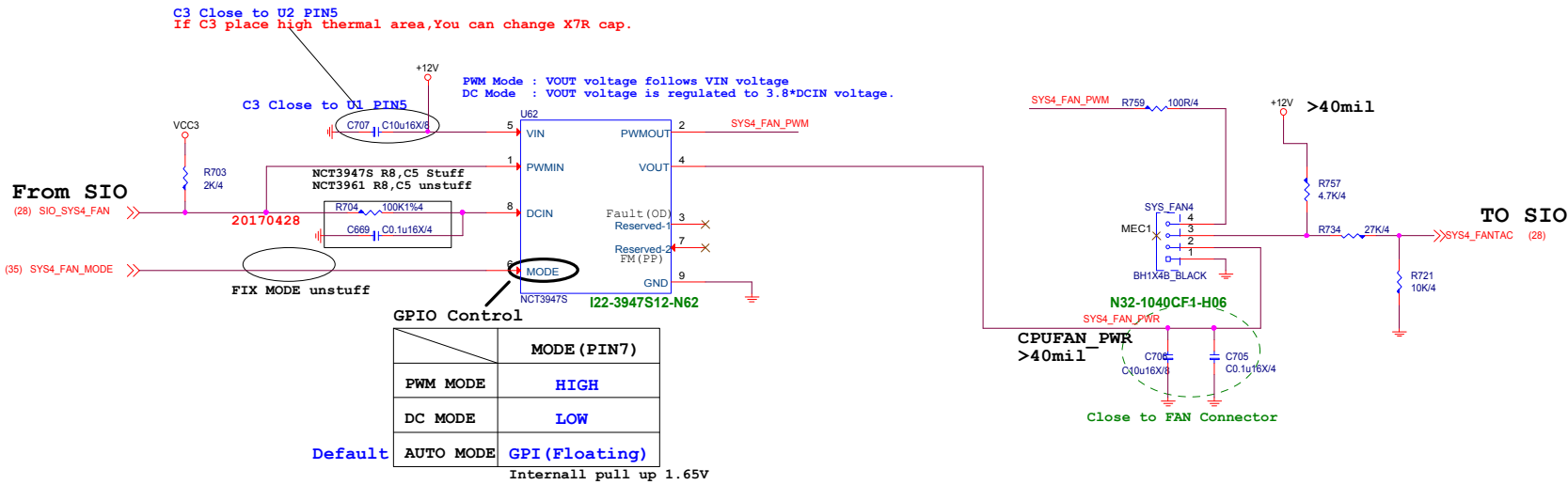
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

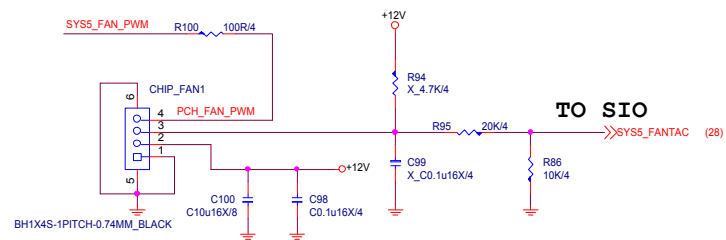
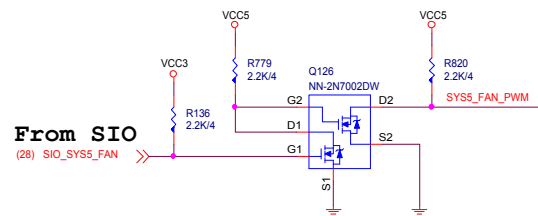
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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PCH_FAN



By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE
Default GPI

BIOS SHOW FAN MODE Information USE
Default GPI

use avoid S5 leakage



By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

slave address :
Write 4CH
Read 4DH



By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT SYS FAN1
GP15	EXT SYS FAN2



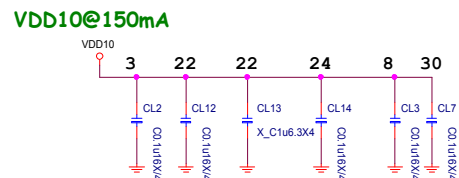
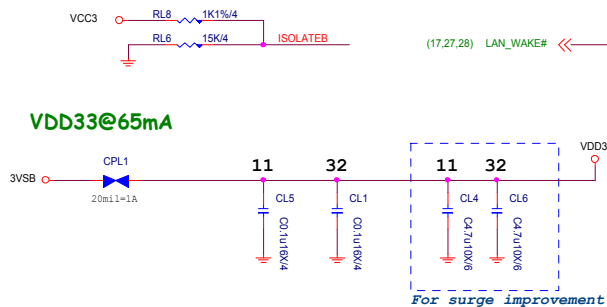
MICRO-STAR INT'L CO.,LTD

MS-7C37

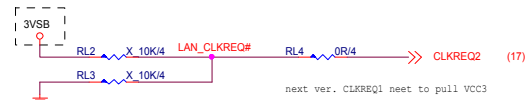
Size	Document Description	Rev
Custom	FAN GPIO NCT5635	1.4
Date: Wednesday, September 25, 2019	Sheet 35 of 75	

RTL8111H Giga LAN

VDD33
RL5 X 1K4 LAN_WAKE#
Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



Pull-up resistor RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

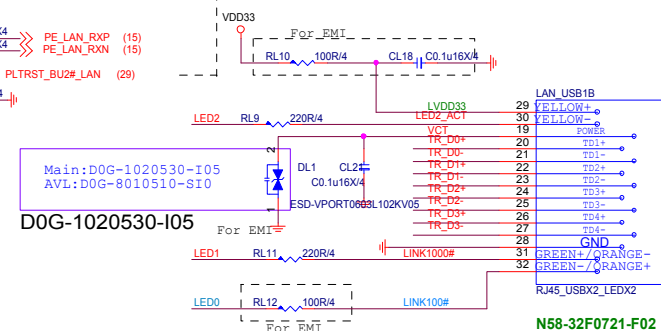


8111H POWER Consumption

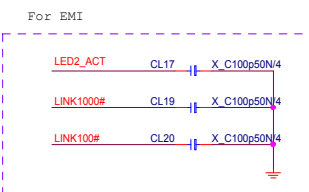
	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#.

LAN Connector

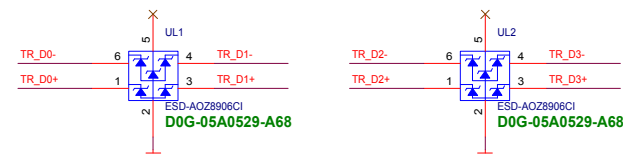


D04-1000201-F07



ESD Protect close to connector

D0G-0200529-A68
D0G-0100619-I05

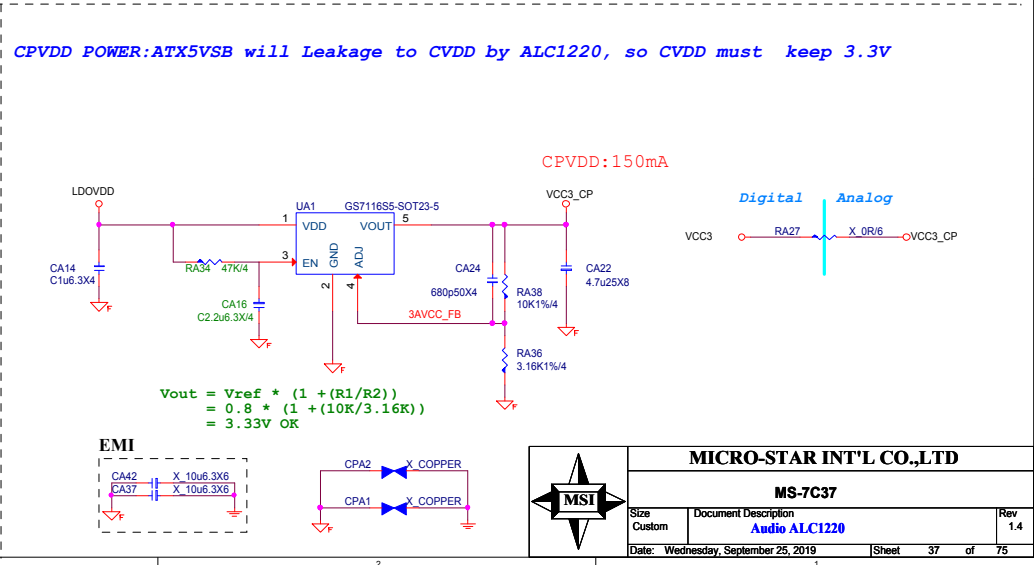
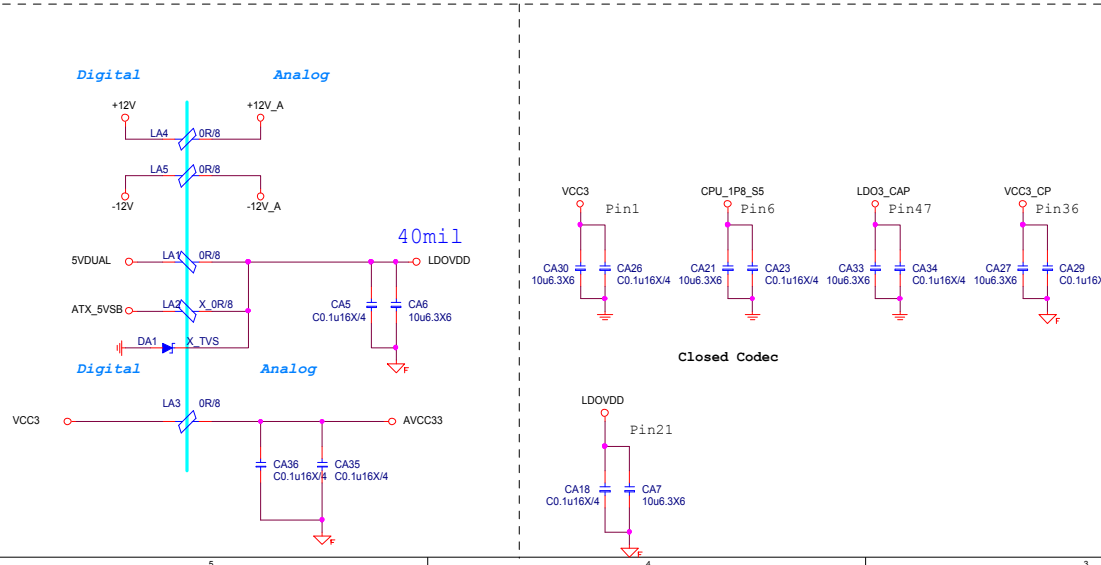
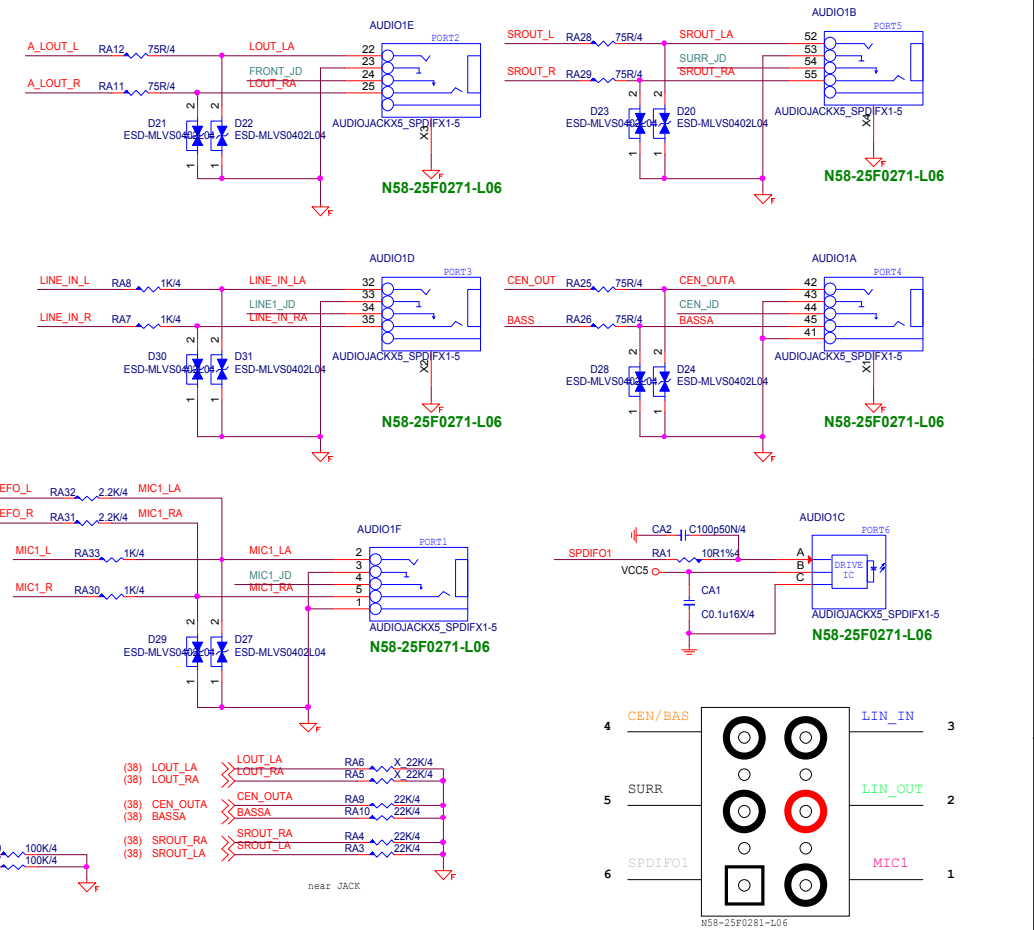
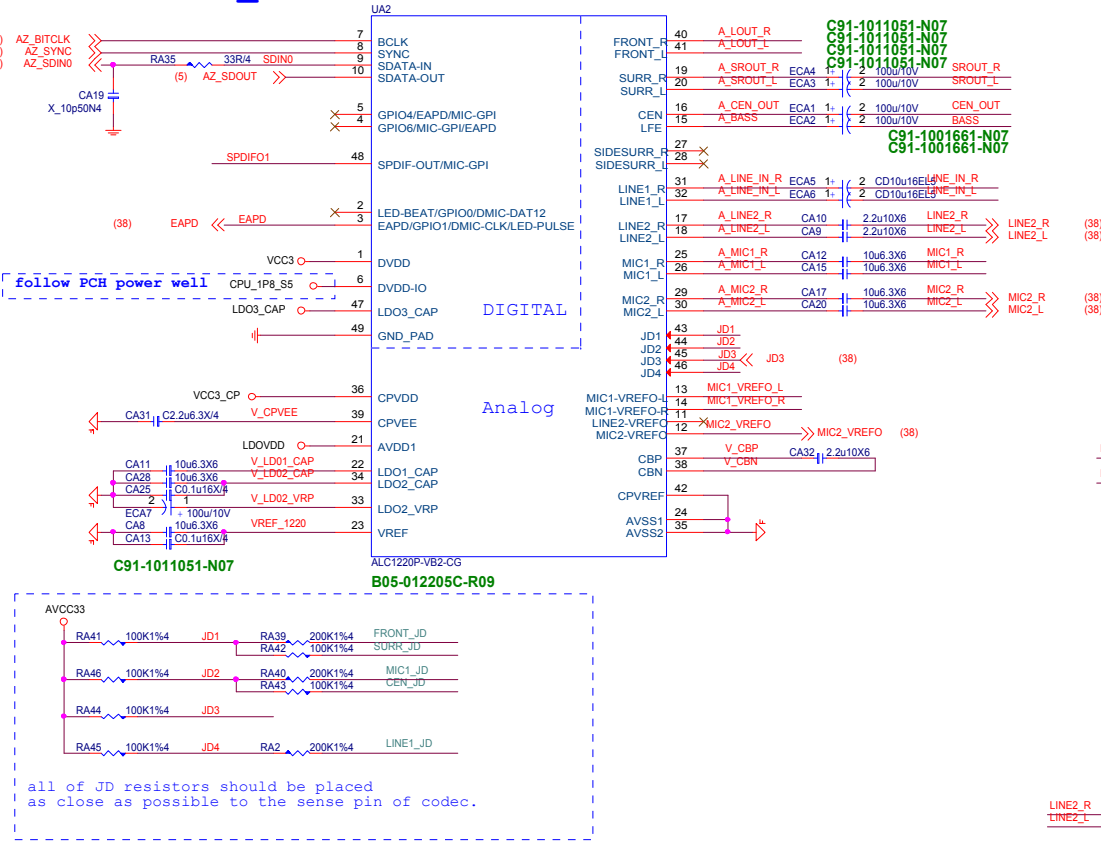


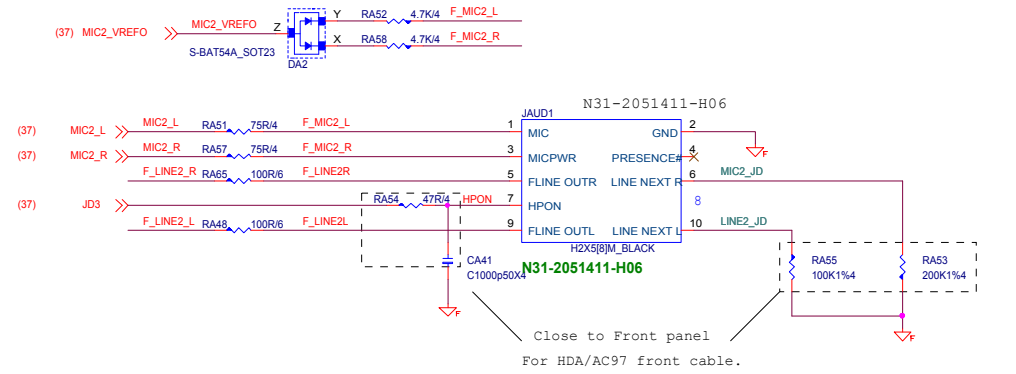
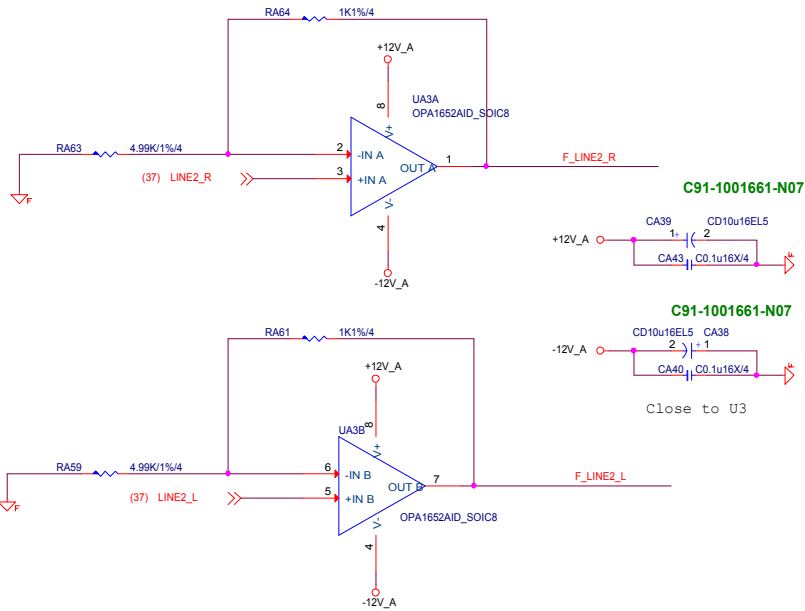
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MS-7C37

Size	Document Description	Rev
Custom	LAN - I211AT	1.4
Date: Wednesday, September 25, 2019	Sheet 36 of 75	

ALC1220P-VB2_48PIN

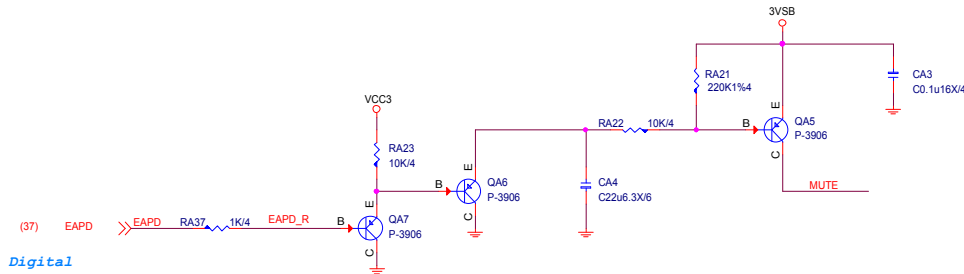




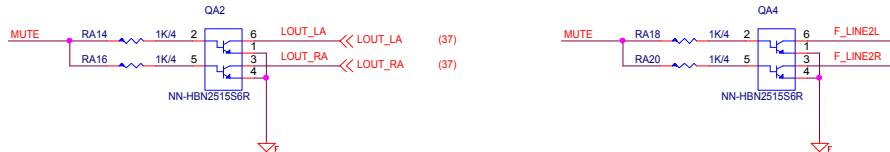
Close to Jack
ESD protect



Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

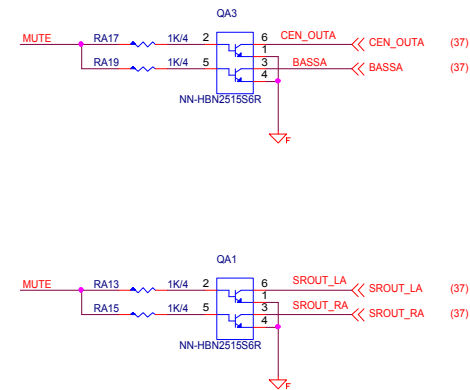


Analog

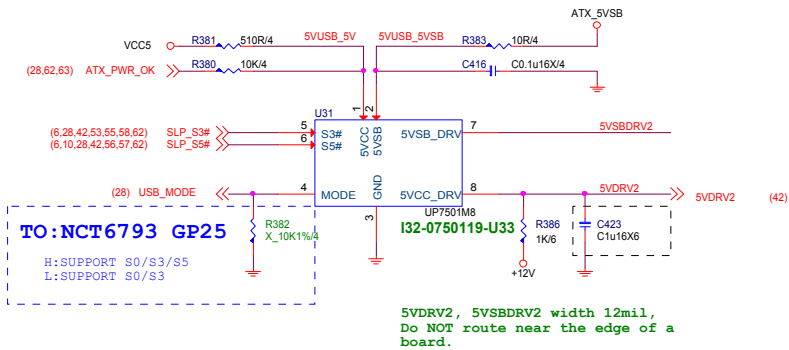


Audio moat is transparent and width 40mil

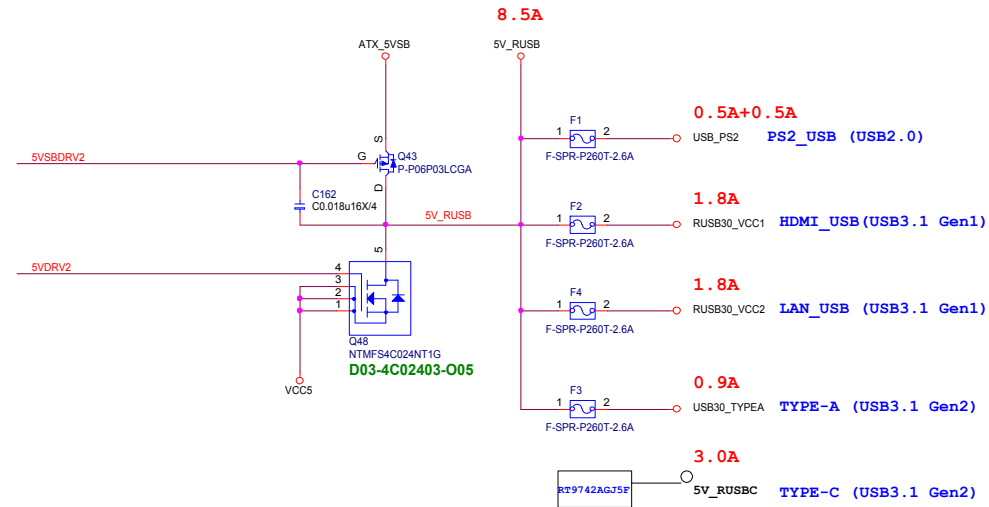
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA, SROUT_RA, CEN_OUTA, BASSA to TVS)



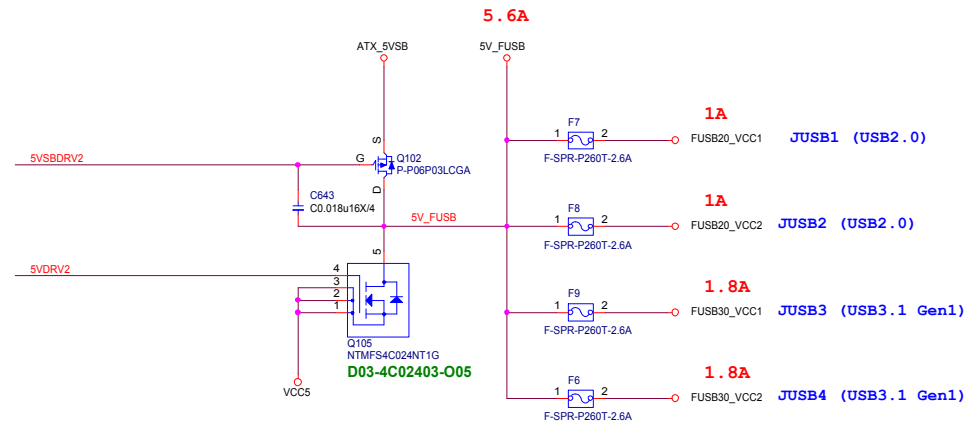
USB Power



Rear USB Port Power



Front USB Port Power



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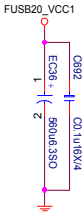
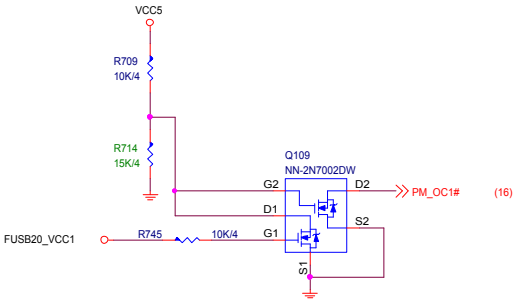
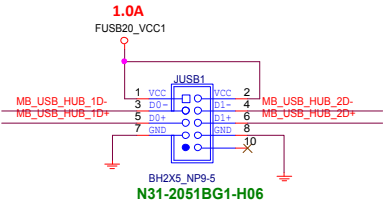
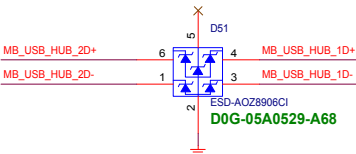


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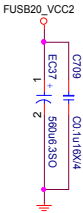
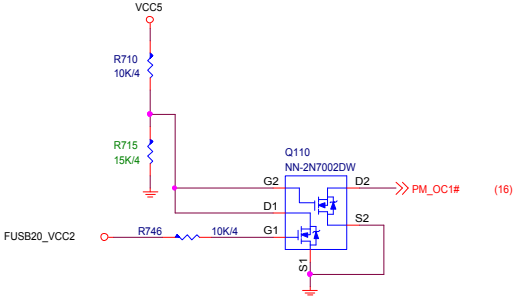
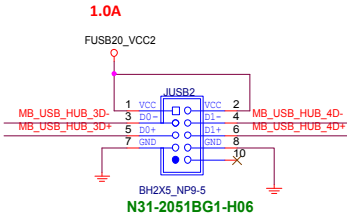
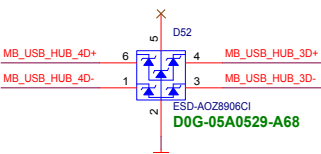
Size Custom	Document Description USB Power - UP7501	Rev 1.4
Date: Wednesday, September 25, 2019		Sheet 39 of 75

Front USB2.0 (JUSB1)



C71-56106R1-N07

Front USB2.0 (JUSB2)



C71-56106R1-N07

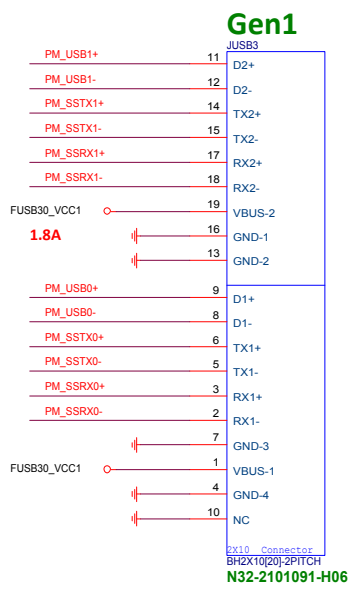
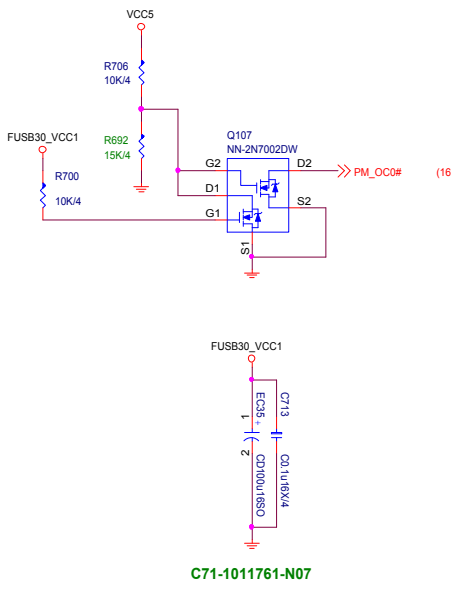
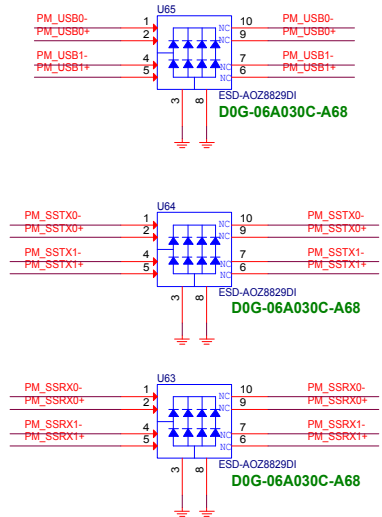
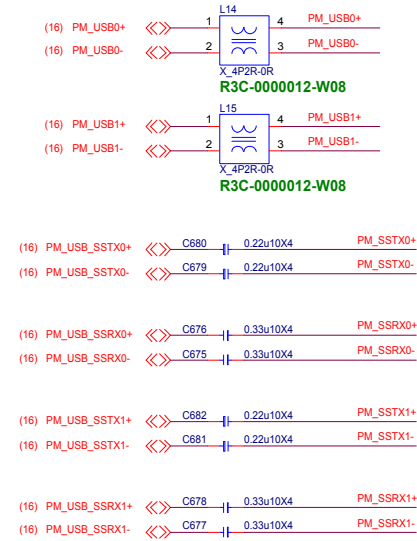


MICRO-STAR INT'L CO.,LTD

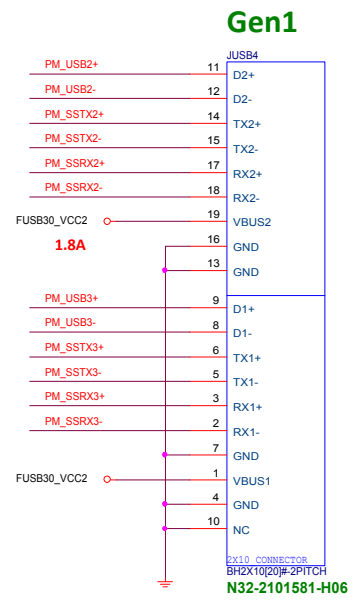
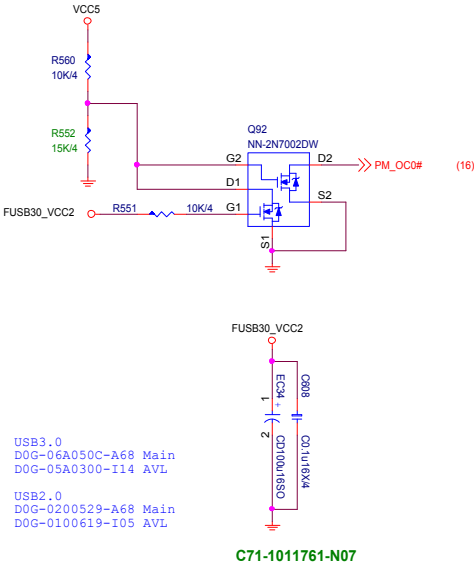
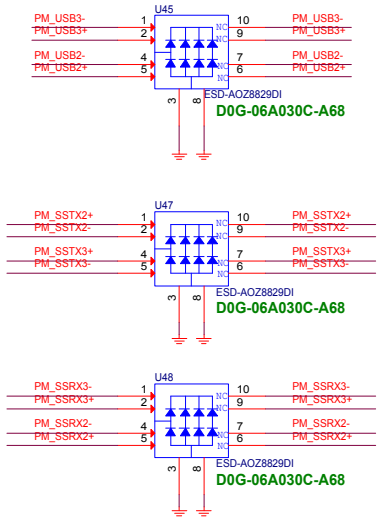
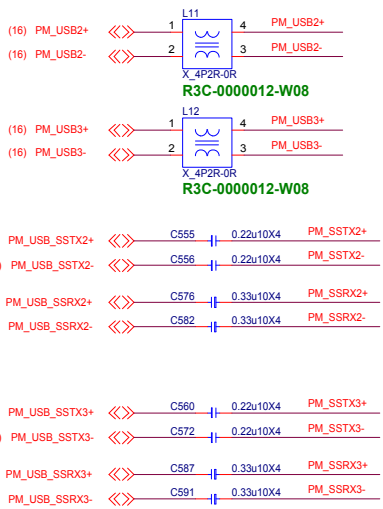
MS-7C37

Size	Custom	Document Description	Front USB2.0 Header	Rev	1.4
Date:	Wednesday, September 25, 2019	Sheet	40	of	75

Front USB3 180° BOX Header(JUSB3)



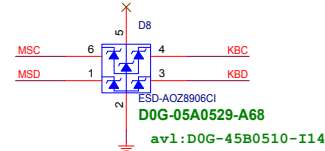
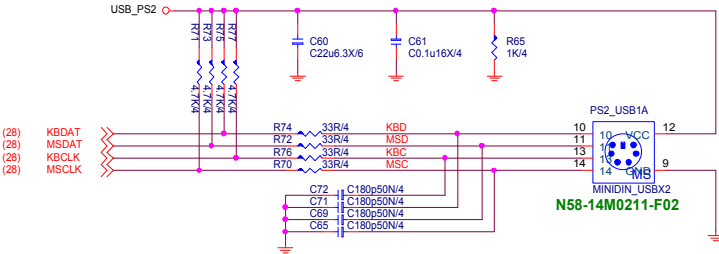
Front USB3 90° BOX Header(JUSB4)



PS2

5V@1A

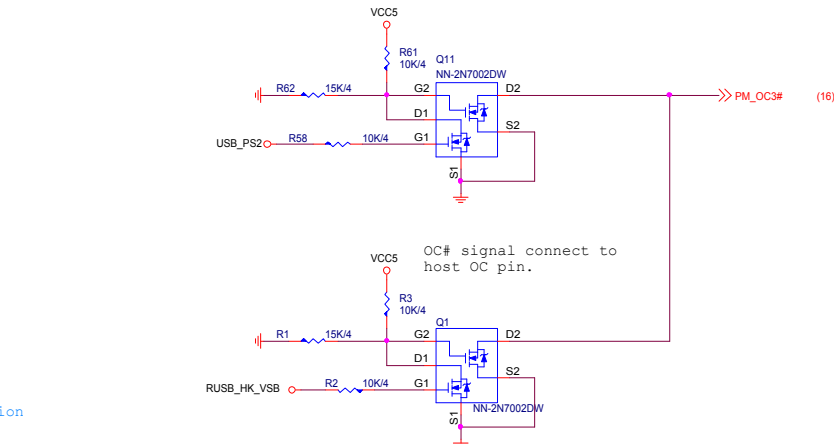
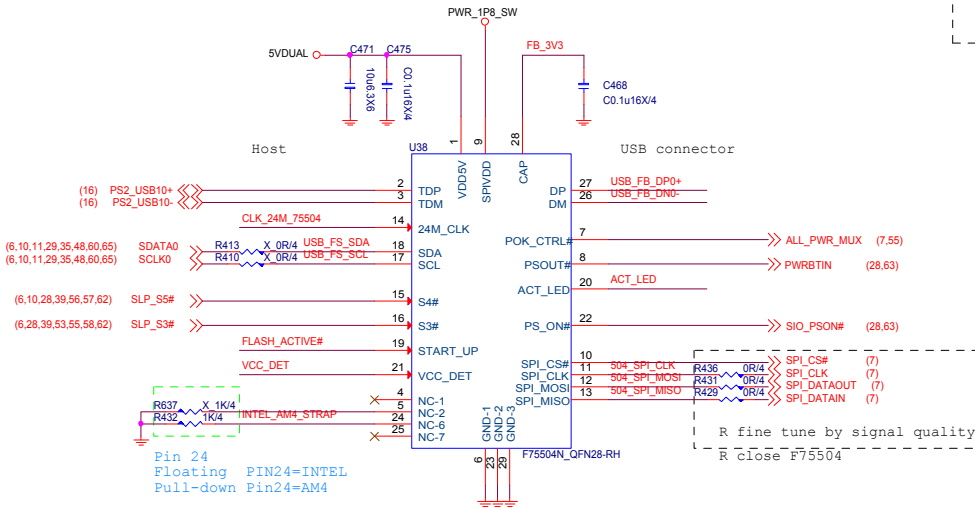
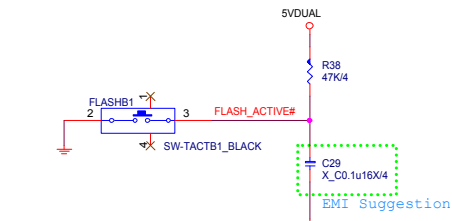
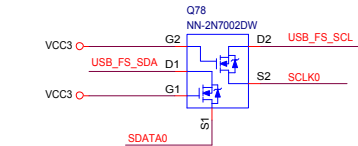
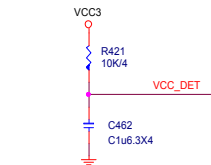
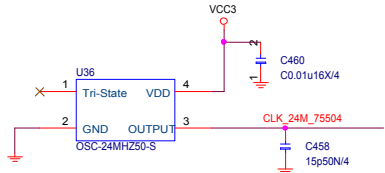
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



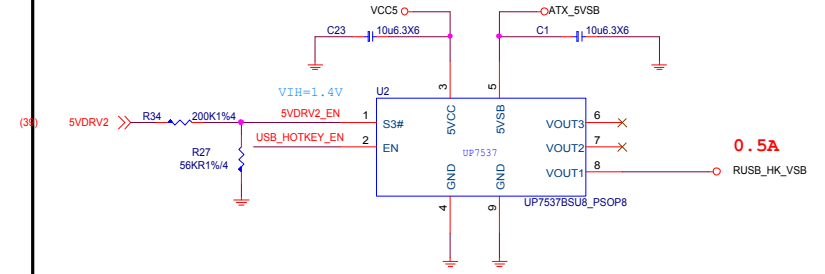
USB2.0 Flash BIOS

F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

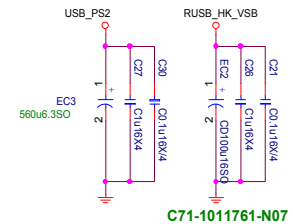
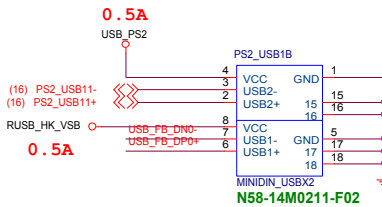
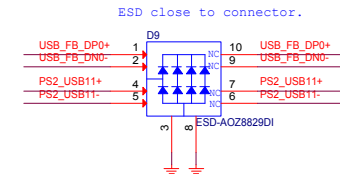
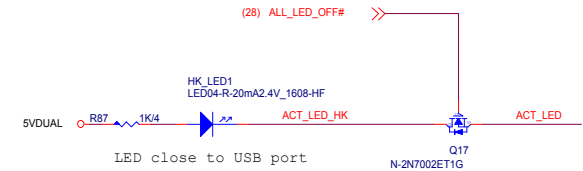
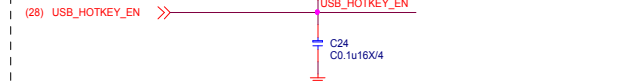
CLK running in S0,don't require in sleep



HOTKEY POWER



default=> GPI
Register POWER Well
=> VSB or VBAT

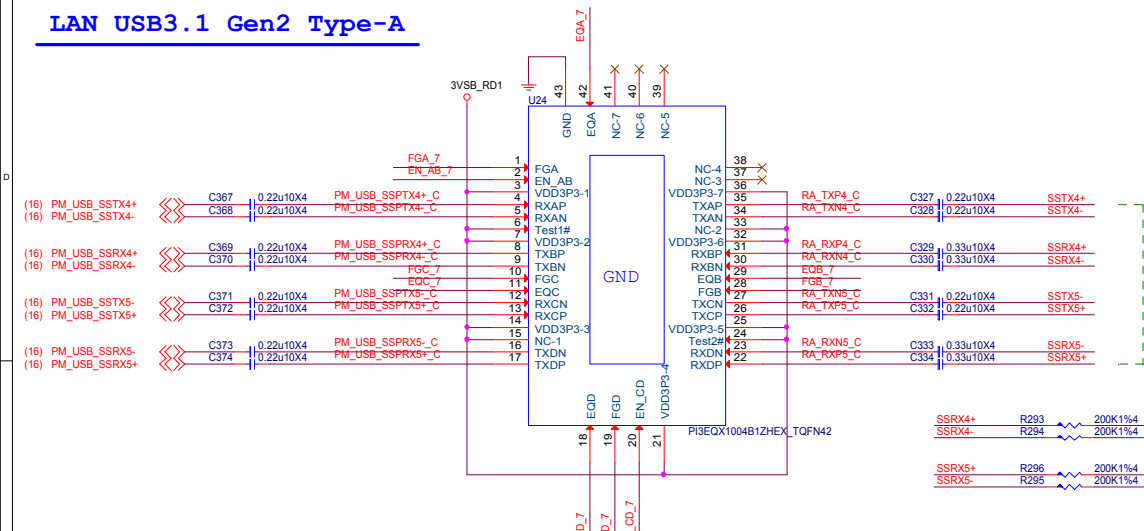


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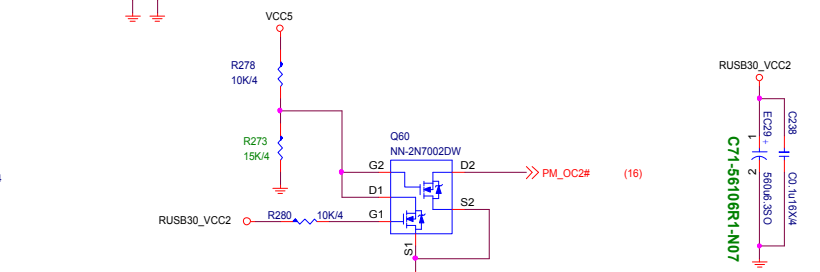
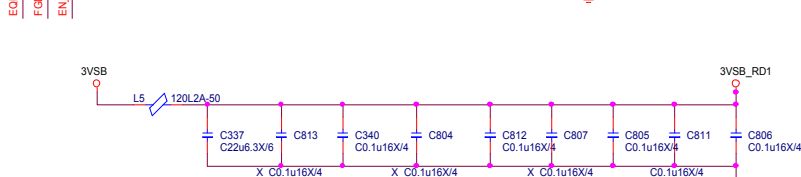
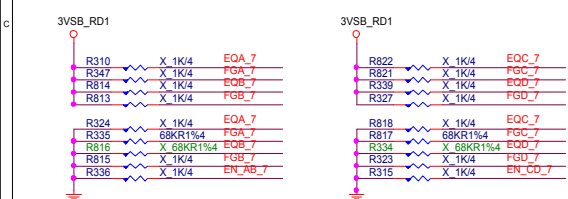
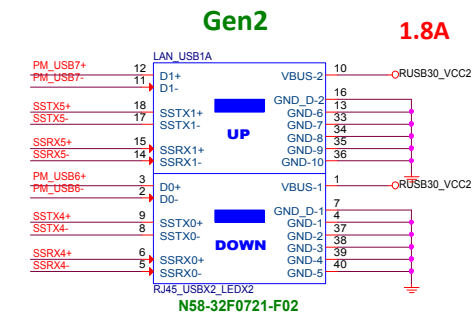
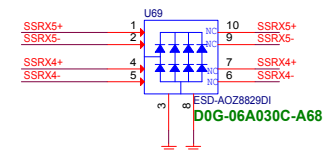
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Size	Document Description	Rev
Custom	Rear USB2.0 + PS2	1.4
Date: Wednesday, September 25, 2019	Sheet 42 of 75	

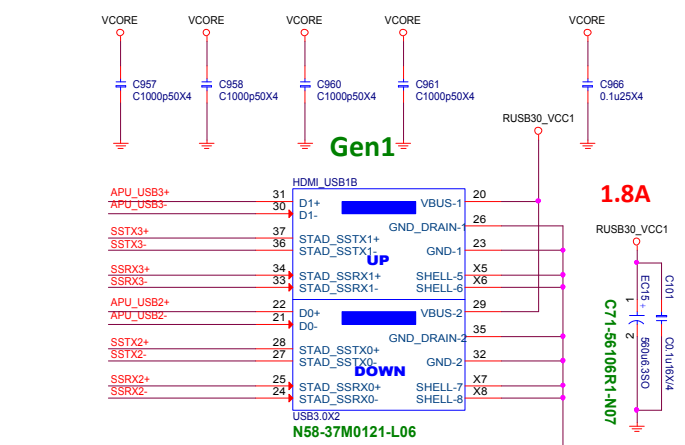
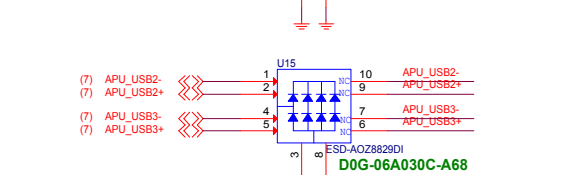
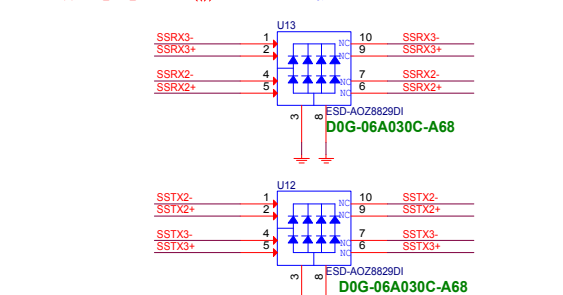
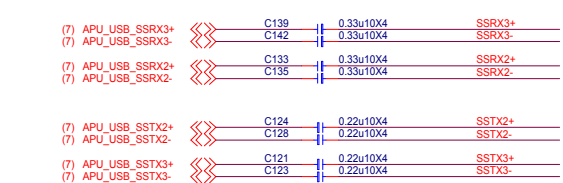
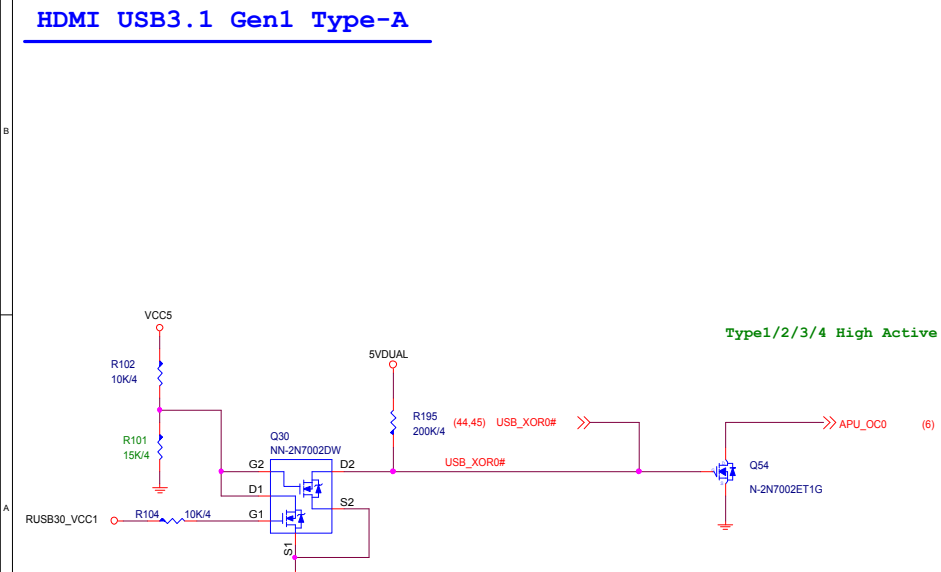
LAN USB3.1 Gen2 Type-A



Rear LAN Type-A



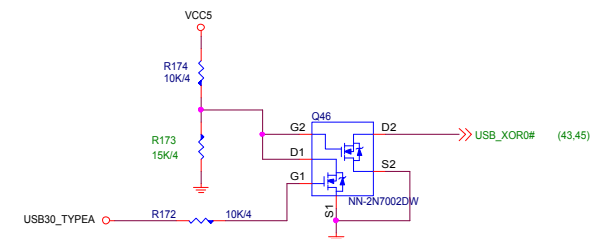
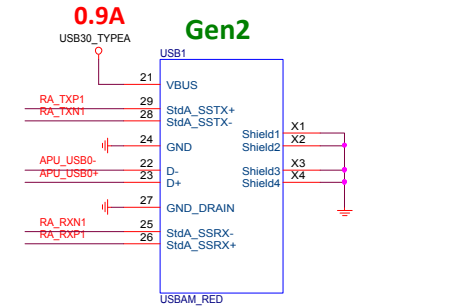
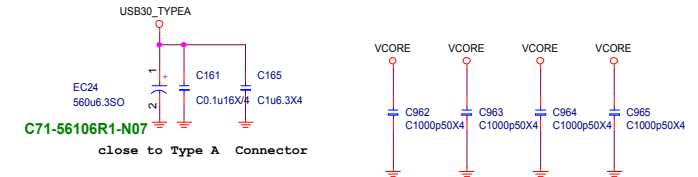
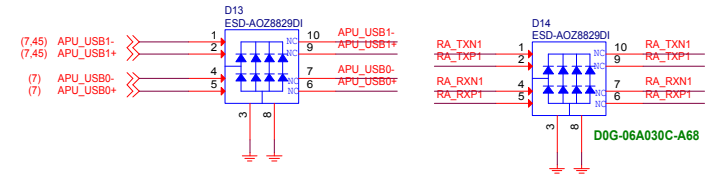
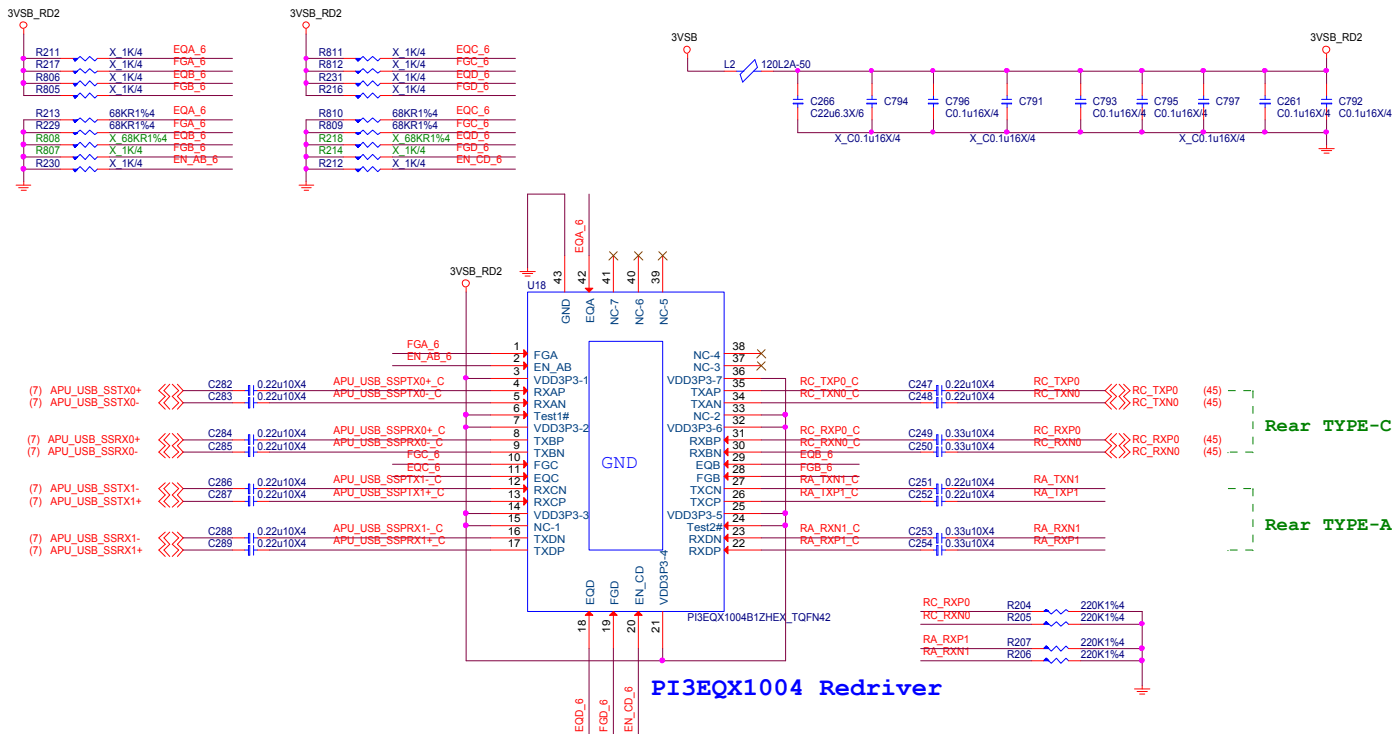
HDMI USB3.1 Gen1 Type-A



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MS-7C37			
Size	Document Description	Rev	
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Date: Wednesday, September 25, 2019	Sheet	43	of 75

USB3.1 Gen2 Redriver + Type-A



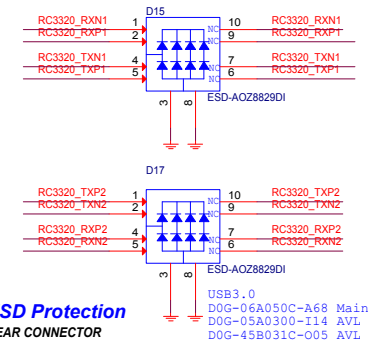
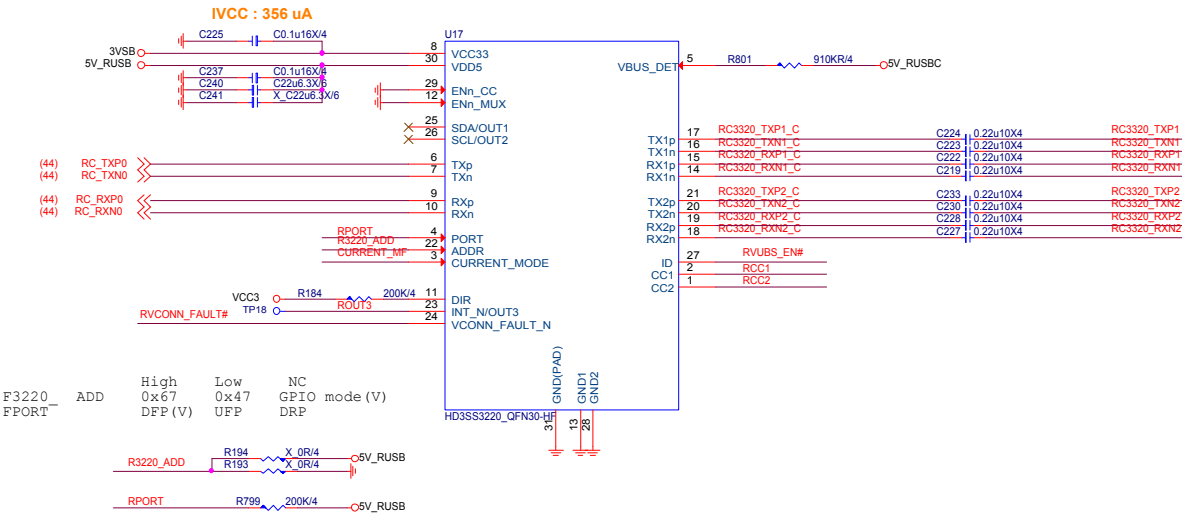
MICRO-STAR INT'L CO.,LTD

MS-7C37

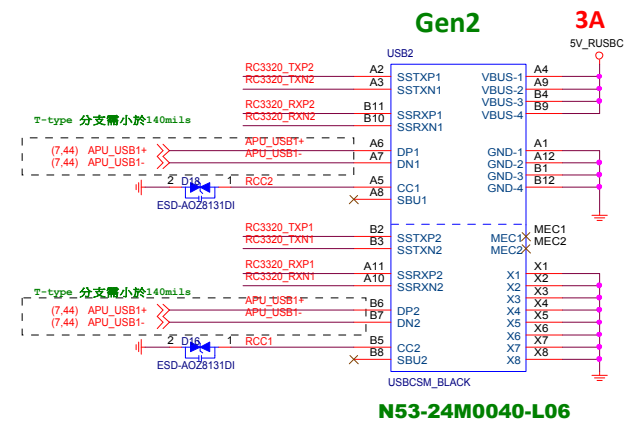
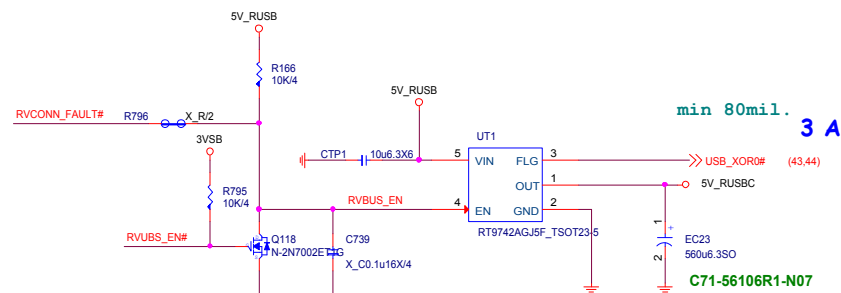
Size Custom	Document Description Rear USB3.1 Type A / redrive	Rev 1.4
Date: Wednesday, September 25, 2019	Sheet 44 of 75	

USB3.1 Gen2 Type-C

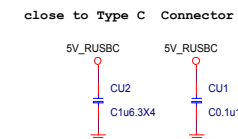
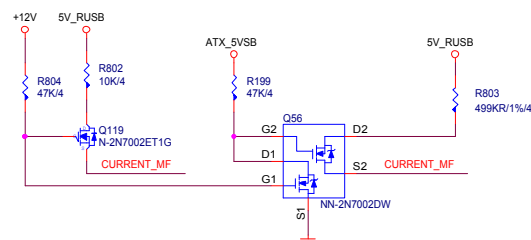
USB Type-C MUX with Configuration Channel (CC)



VBUS EN



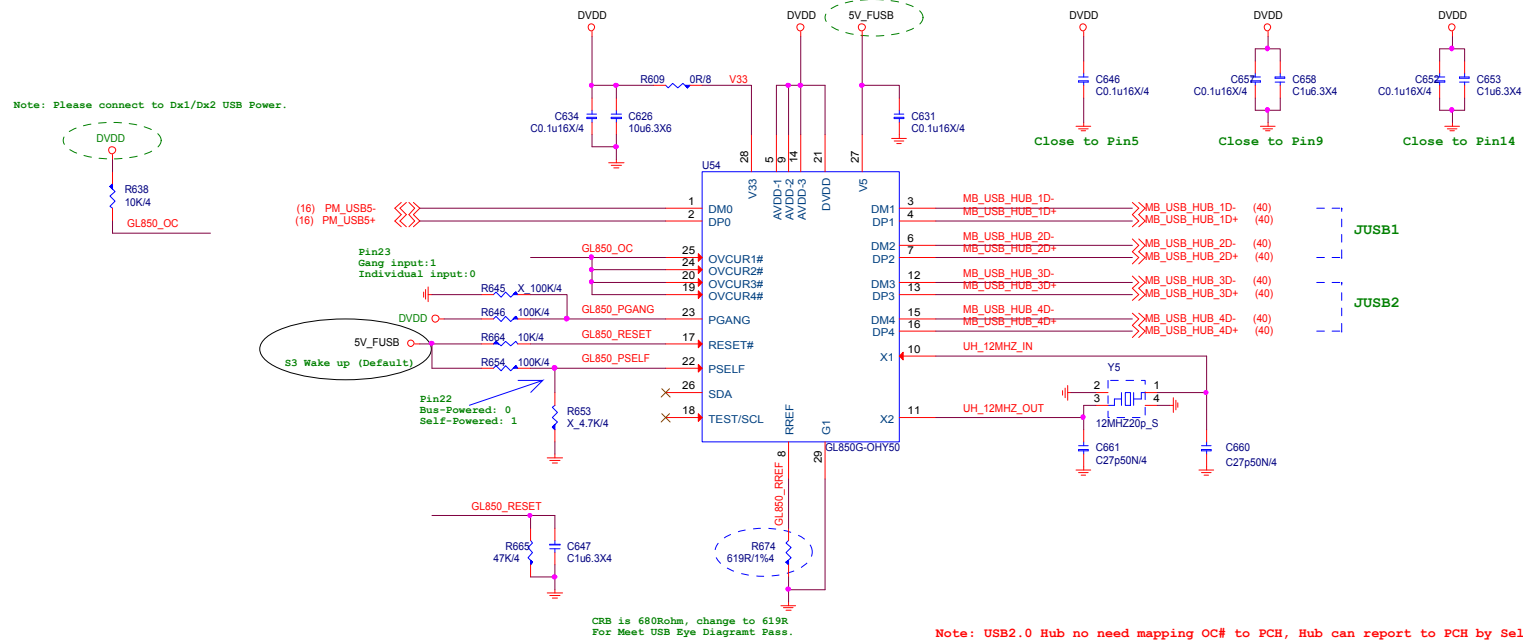
Current Mode



GL850G USB2.0 HUB

5V_FUSB

Note: Please connect to USB Power Source



Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

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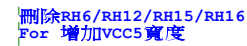


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For HDMI 1.4



AUX Level Shifter



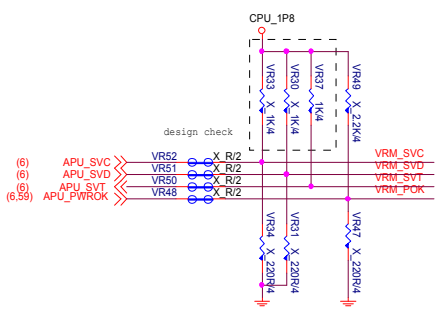
Pin connection diagram for D0G-06A030C-A68. The diagram shows a 10-pin connector with pins 1 through 10. Pins 1, 2, 3, 4, and 5 are connected to HDMI_DDC_CLK, HDMI_DDC_DATA, HDMI_HOT_DET, and two ground pins (pins 6 and 7) respectively. Pins 10, 9, 8, 7, and 6 are connected to HDMI_DDC_CLK, HDMI_DDC_DATA, and two ground pins (pins 11 and 12) respectively. The component is labeled D0G-06A030C-A68.



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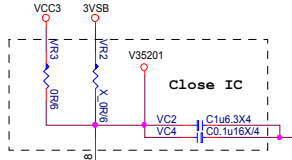
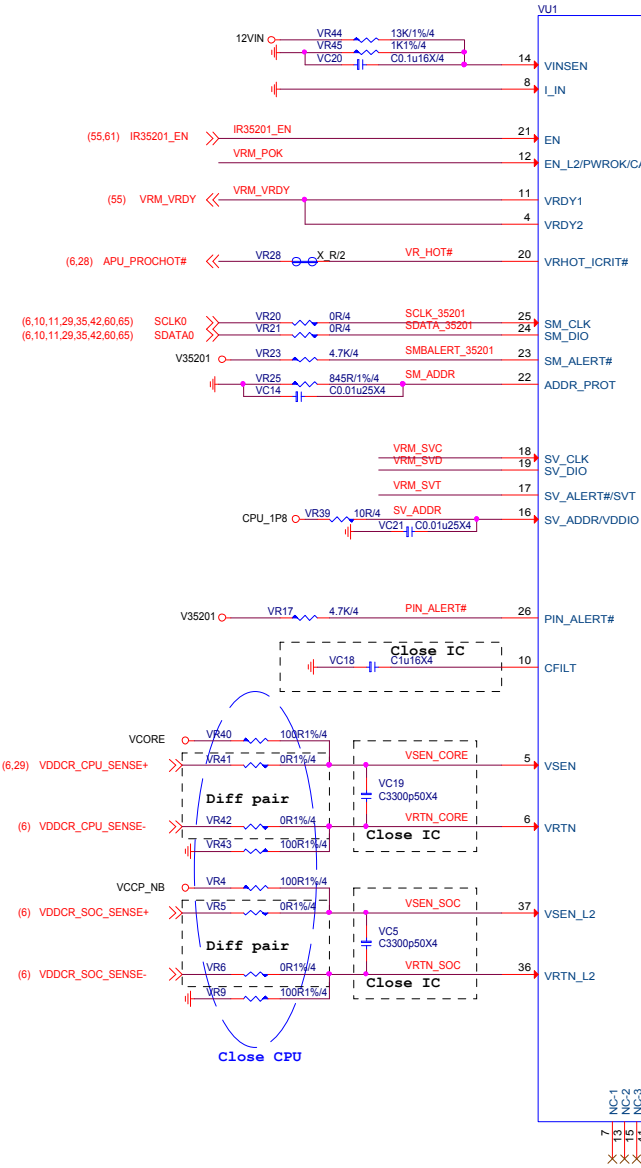
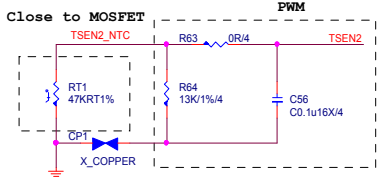
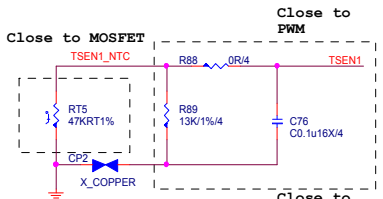
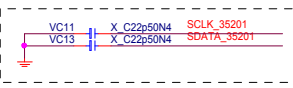
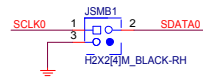
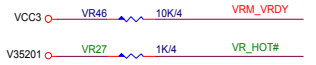
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Size Custom	Document Description HDMI	Rev 1.4
Date: Wednesday, September 25, 2019		Sheet 47 of 75

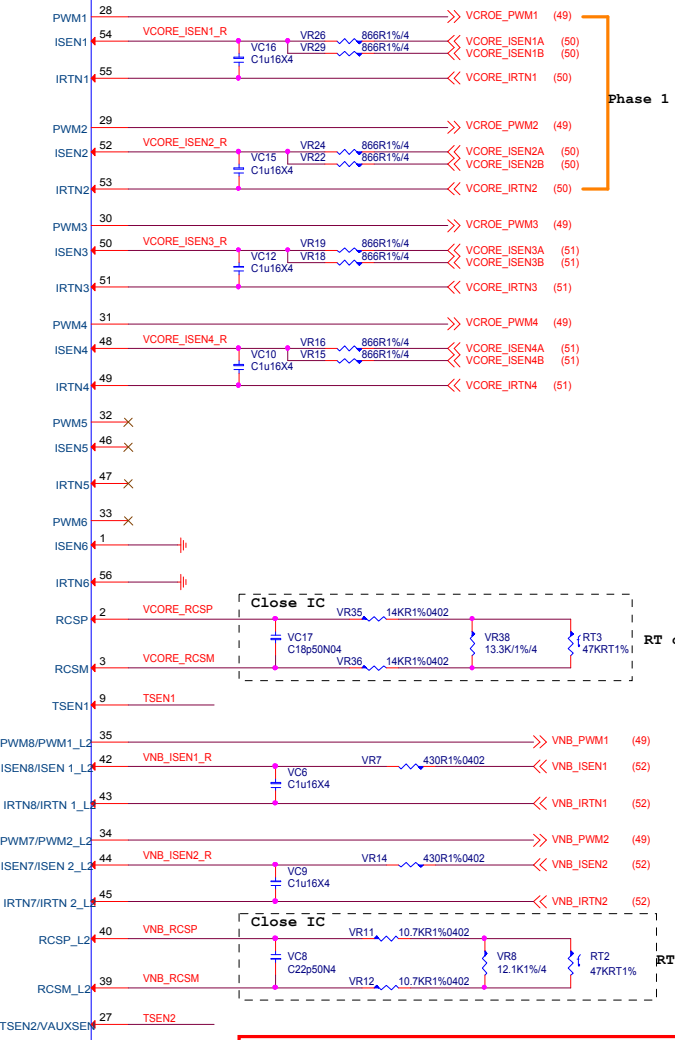


Note:VID Override Circuit

BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



燒錄打點:IC正面上橋+金色點



VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 192A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 90A

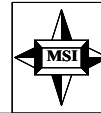
Phase 1 close to CPU power pin.

RT close to Choke

RT close to Choke

0x26: RH=18K, RL=13K

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

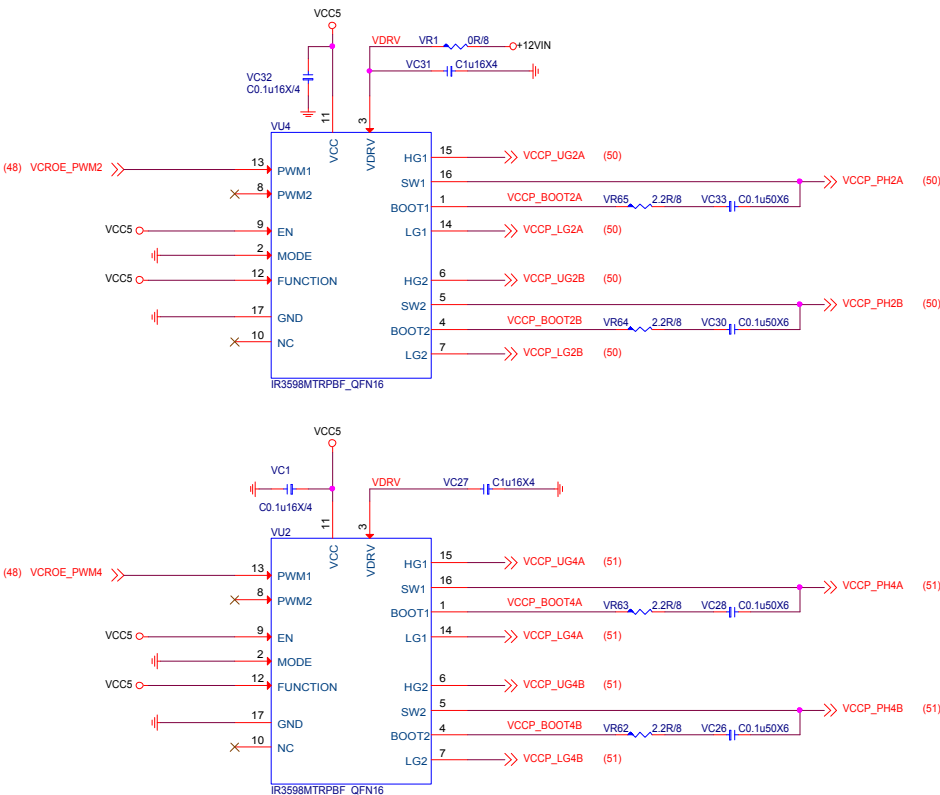
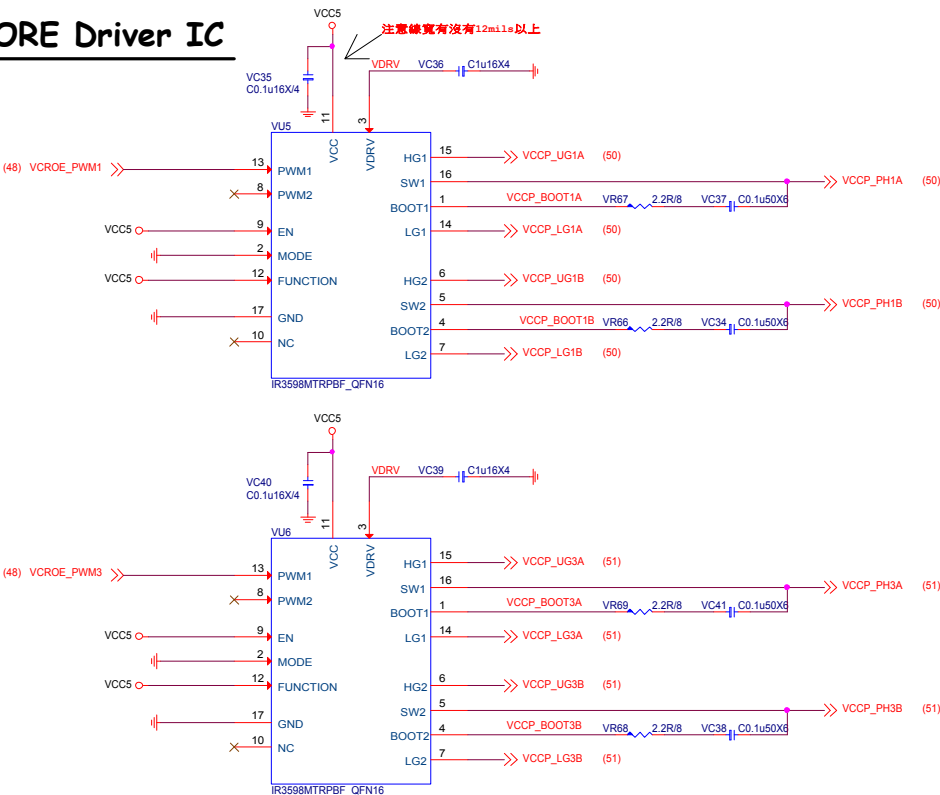


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power IR35201 8+2	1.4
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CPU_CORE Driver IC



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CPU_SOC Driver IC

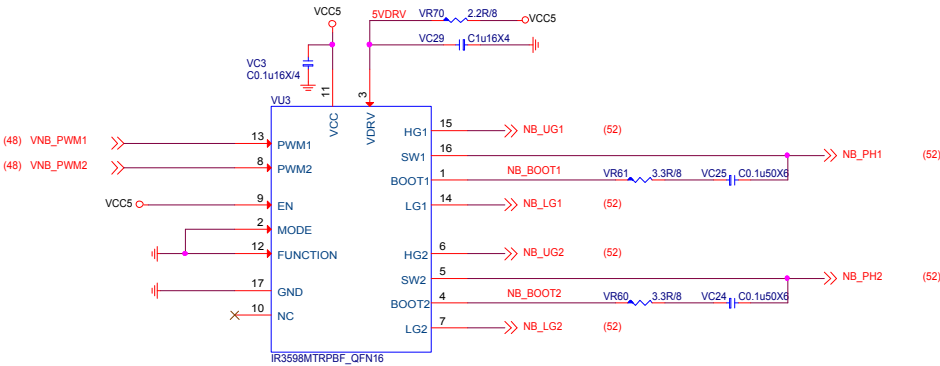


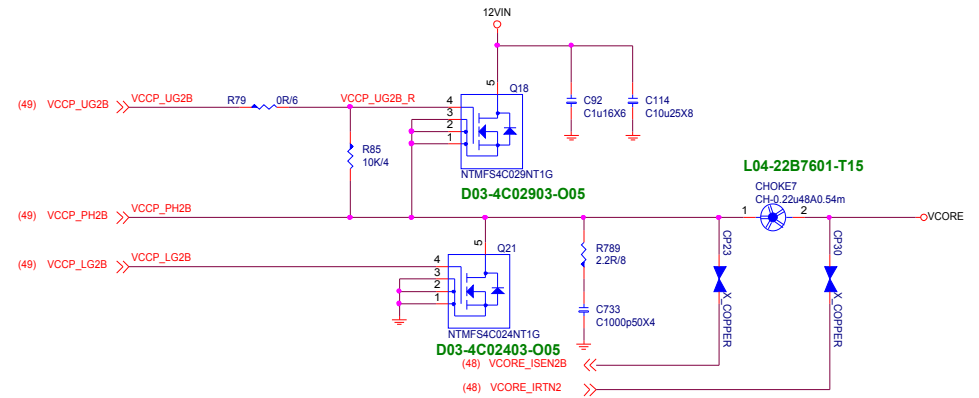
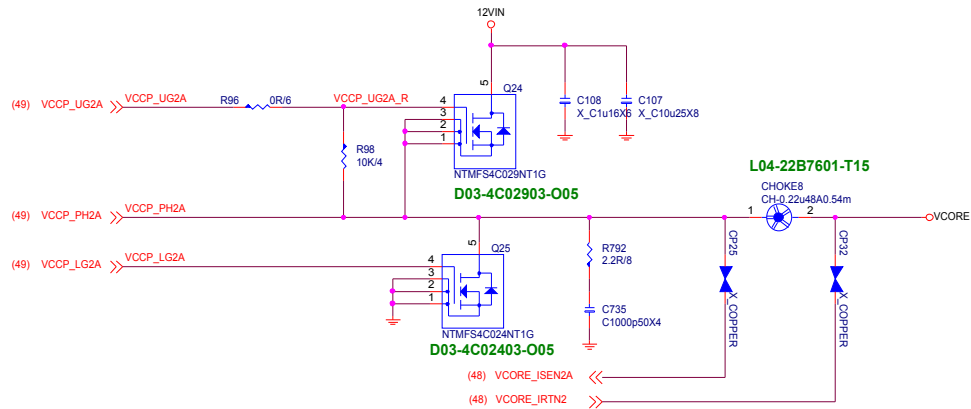
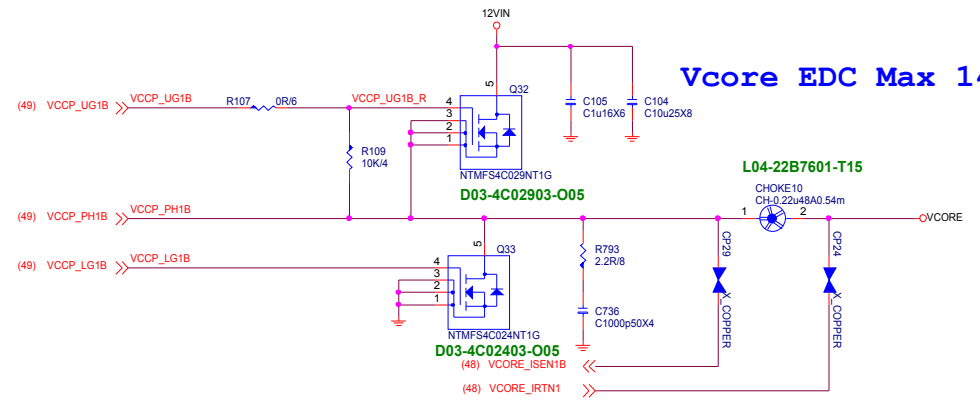
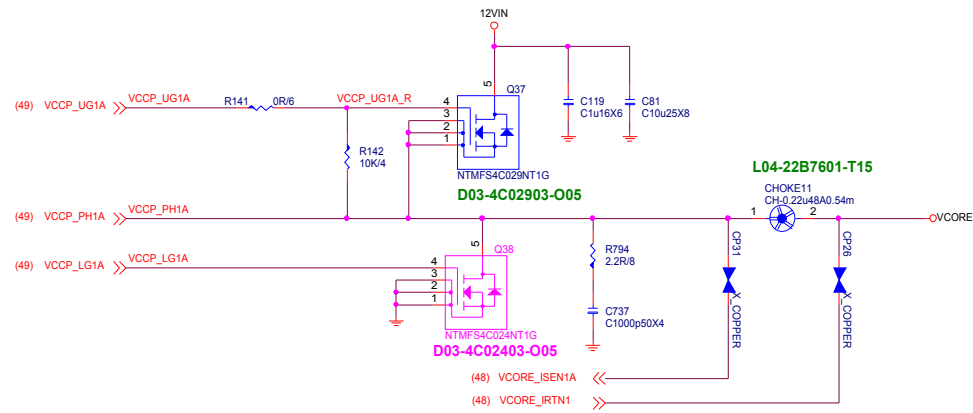
Table for IR3598

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler

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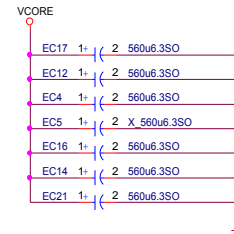
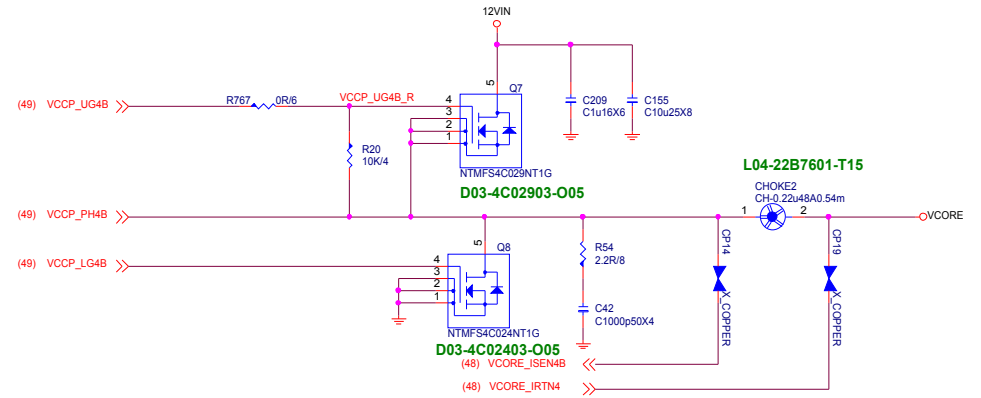
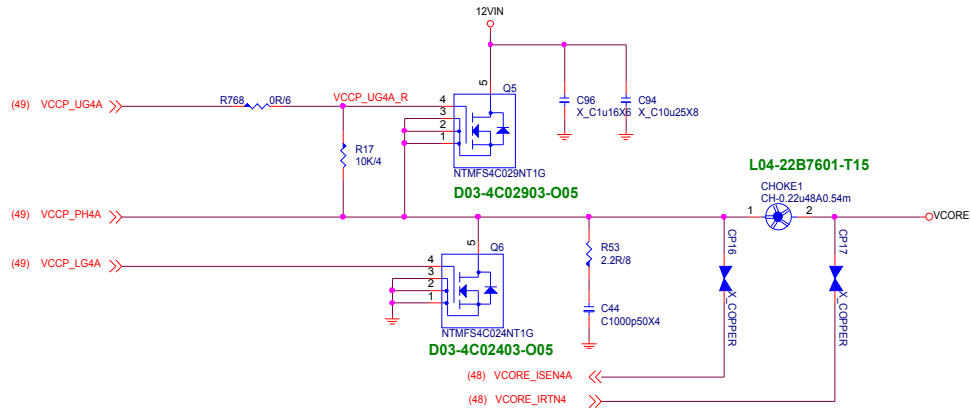
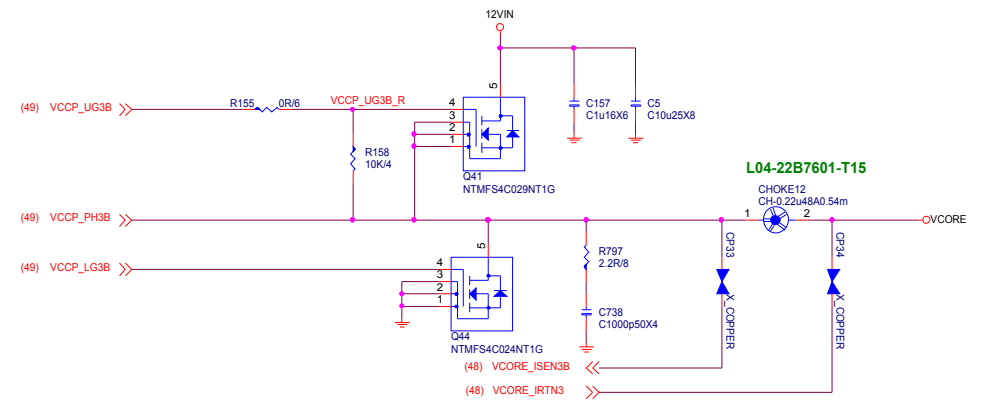
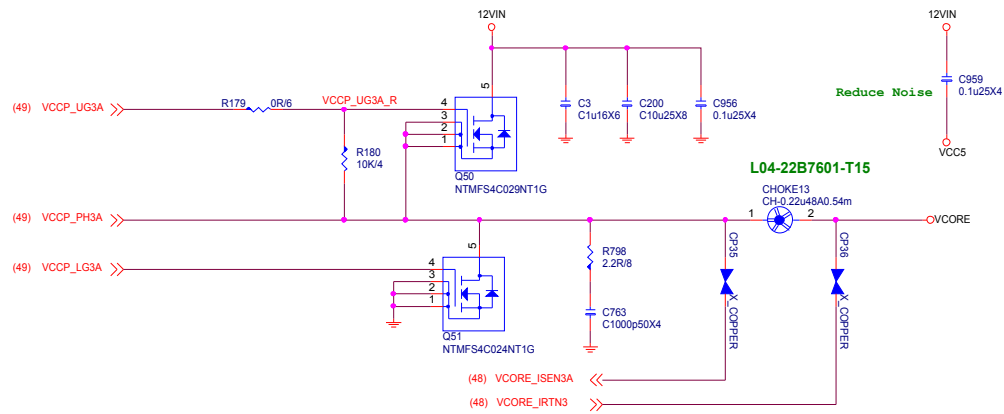
Size	Document Description	Rev
Custom	CPU Power Driver IC IR3598	1.4
Date:	Wednesday, September 25, 2019	Sheet 49 of 75



MICRO-STAR INT'L CO.,LTD

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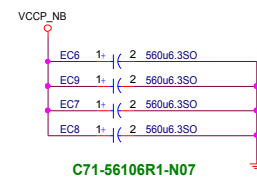
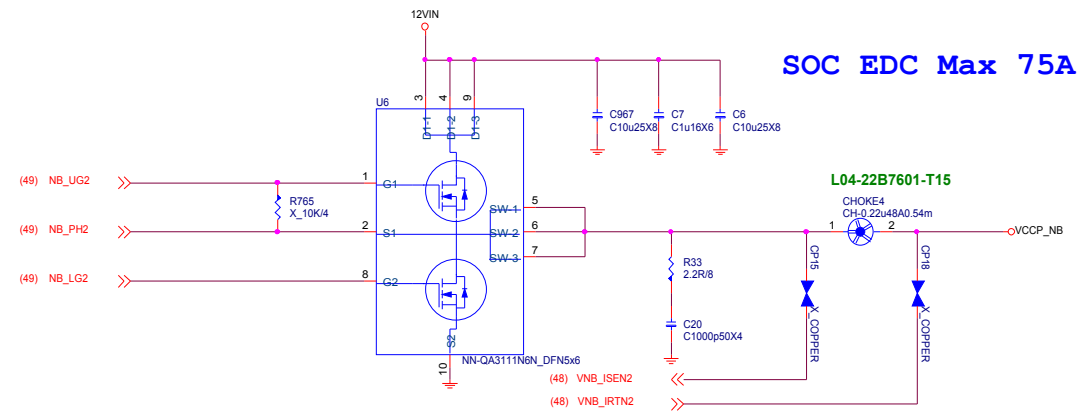
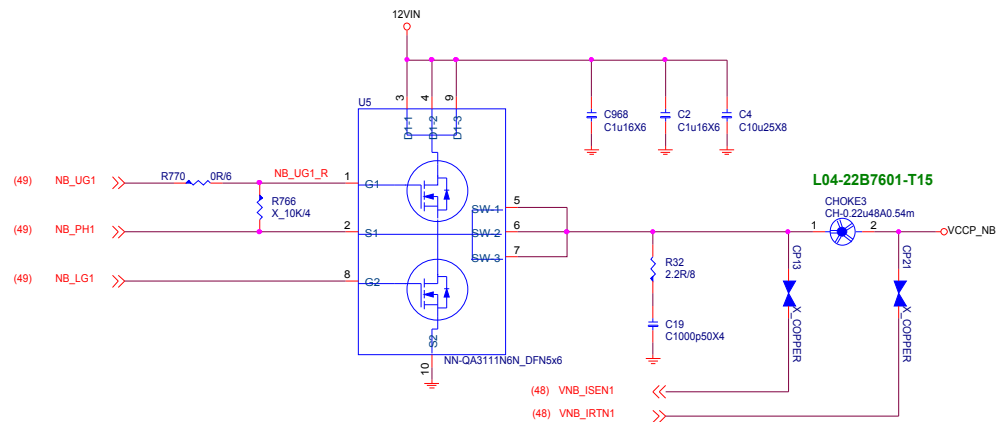
Size	Document Description	Rev
Custom	CPU Power Vcore Phase 1-6	1.4
Date: Wednesday, September 25, 2019	Sheet 50 of 75	



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Size	Document Description	Rev
Custom	CPU Power Vcore Phase 7 - 10	1.4
Date: Wednesday, September 25, 2019	Sheet 51 of 75	



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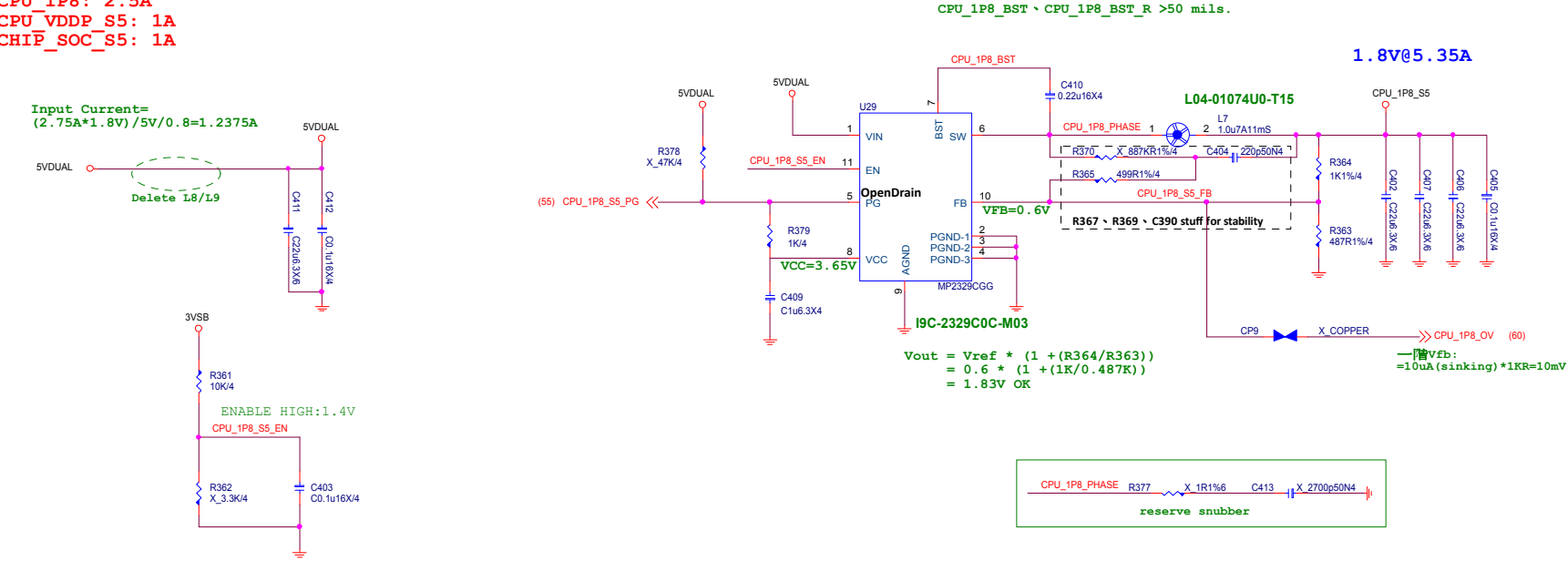
MS-7C37

Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	1.4
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CPU 1P8V S5

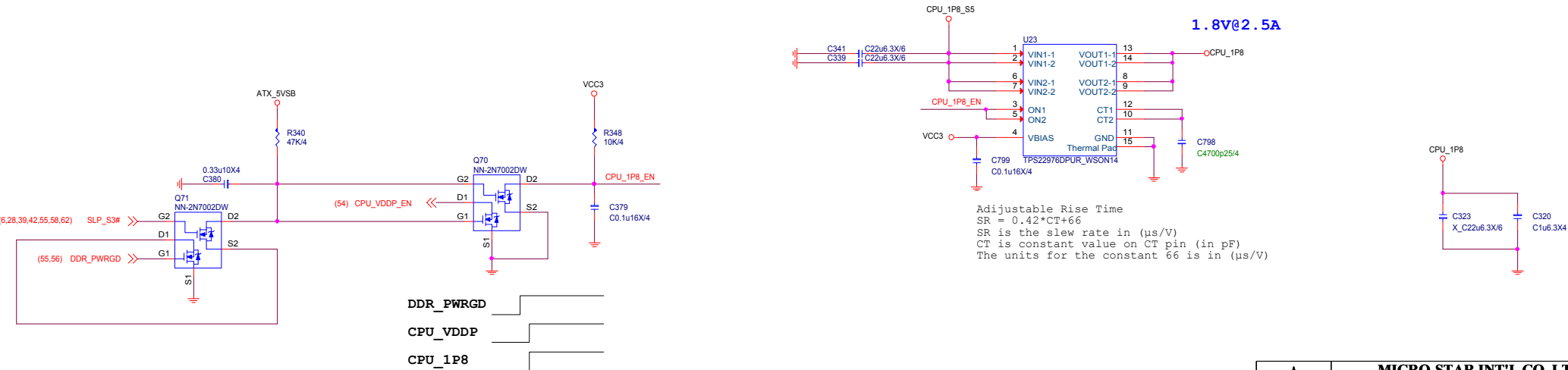
CPU: VDD 18 S5@0.5A
CPU: VDDIO Audio@0.25A
CHIP: VDD_I8_S5@0.1A

CPU_1P8: 2.5A
CPU_VDDP S5: 1A
CHIP_SOC_S5: 1A



CPU 1P8V

CPU: VDD 18@2A
CHIP: VDD_18@0.5A



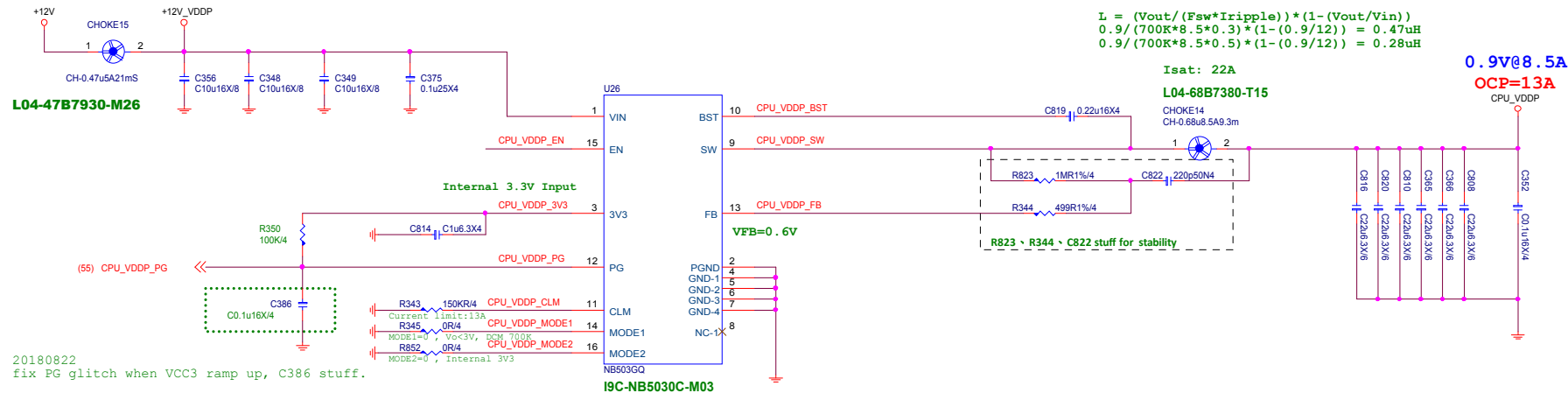
MICRO-STAR INT'L CO.,LTD

MS-7C37

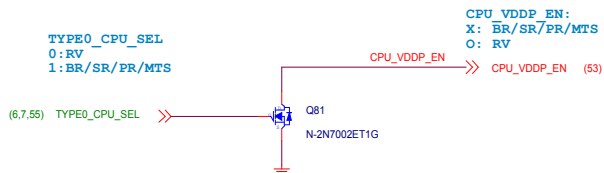
Size	Document Description	Rev
Custom	CPU Power 1.8_S0 / S5	1.4
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CPU: VDDP@8.5A

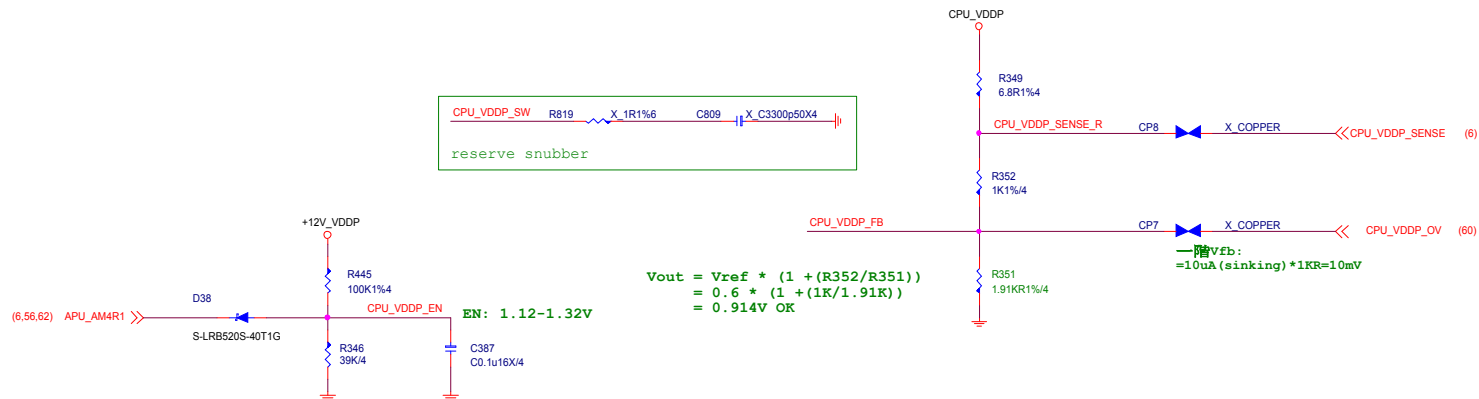
```
Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT( (Vo/Vi) *(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms = 5 A
```



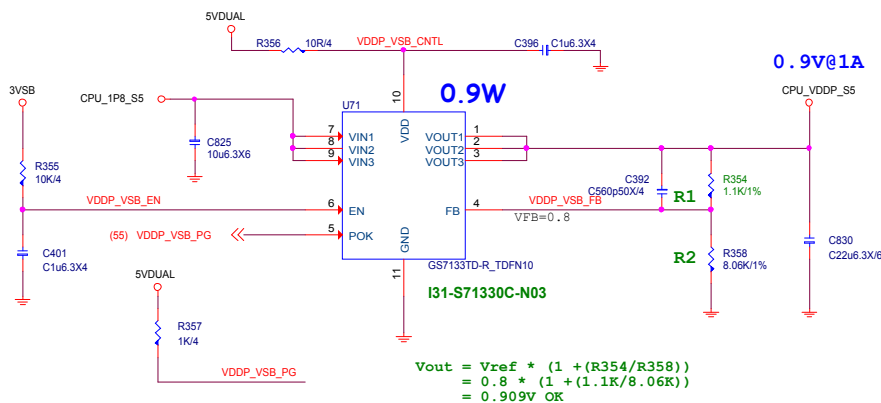
No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE0_CPU_SEL	CPU_VDDP_EN
BR	0	1		0
NA		0	0	0
SR	2	1		0
RV/ZP	3	0	1	1
MTS	4	1		0



CPU: VDDP S5@1A



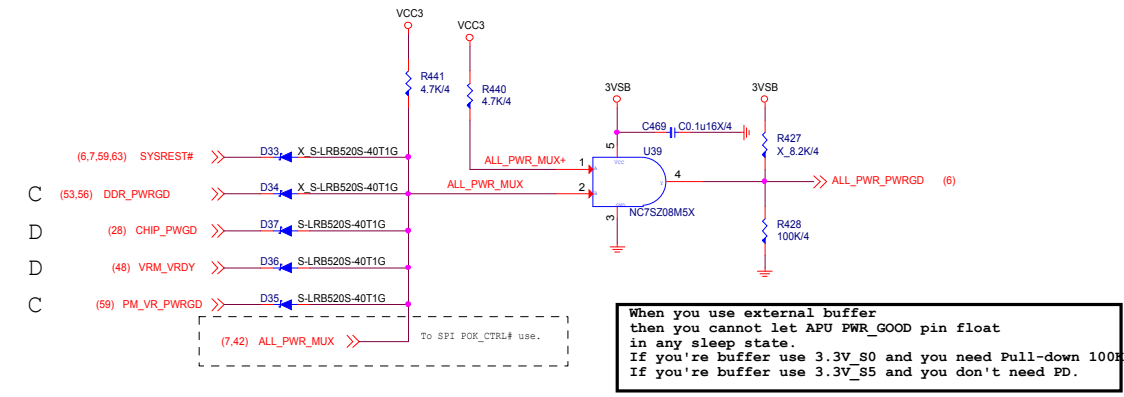
MICRO-STAR INT'L CO.,LTD

MS-7C37

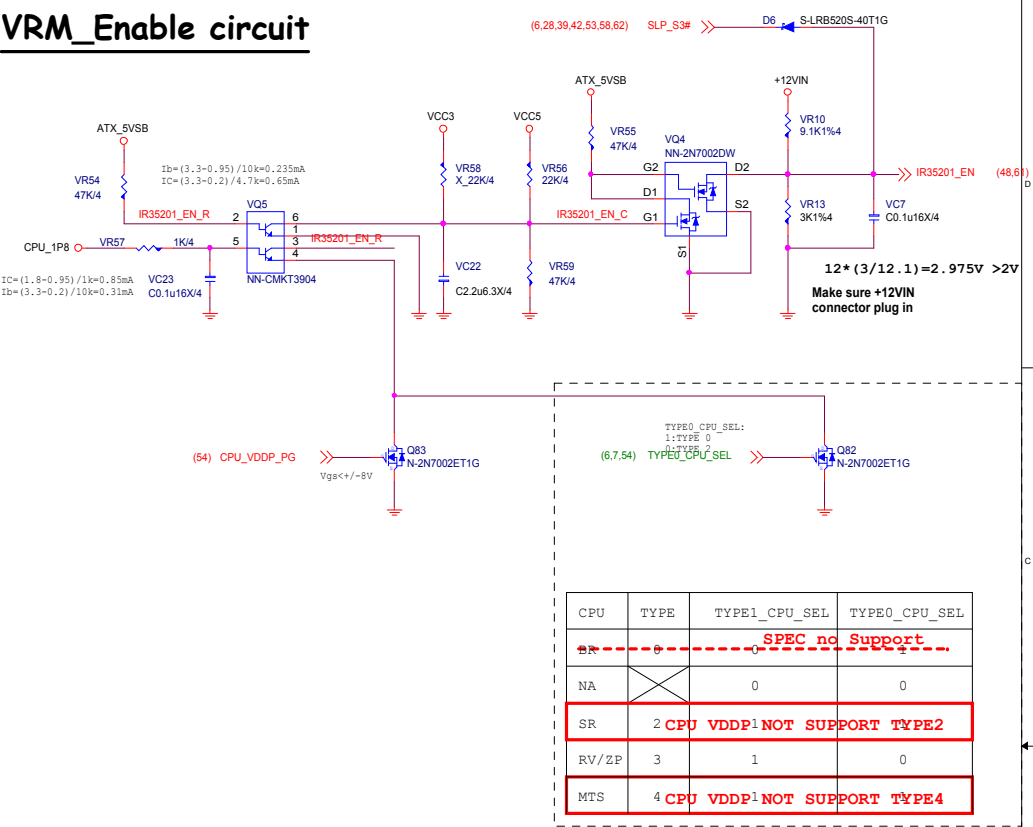
Size Custom	Document Description CPU Power VDDP - NB503	Rev 1.4
Date: Wednesday, September 25, 2019		Sheet 54 of 75

ALL POWER GOOD MUX

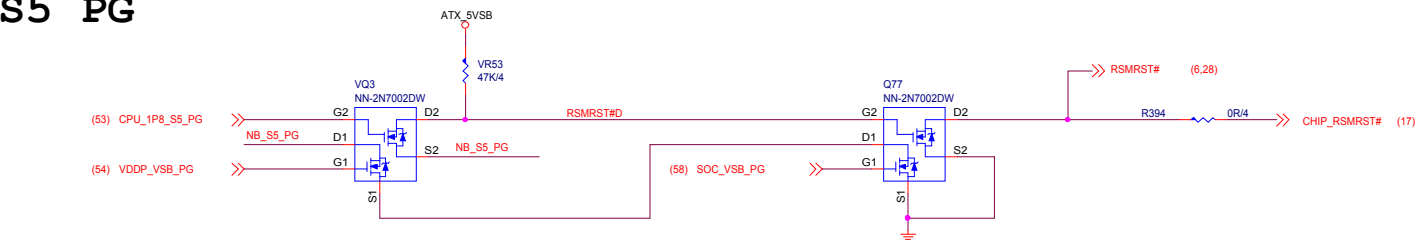
S0 PG



VRM_Enable circuit



S5 PG



15.5A For CPU
9.5A For 4DIMM
1.2A For DDR VTT

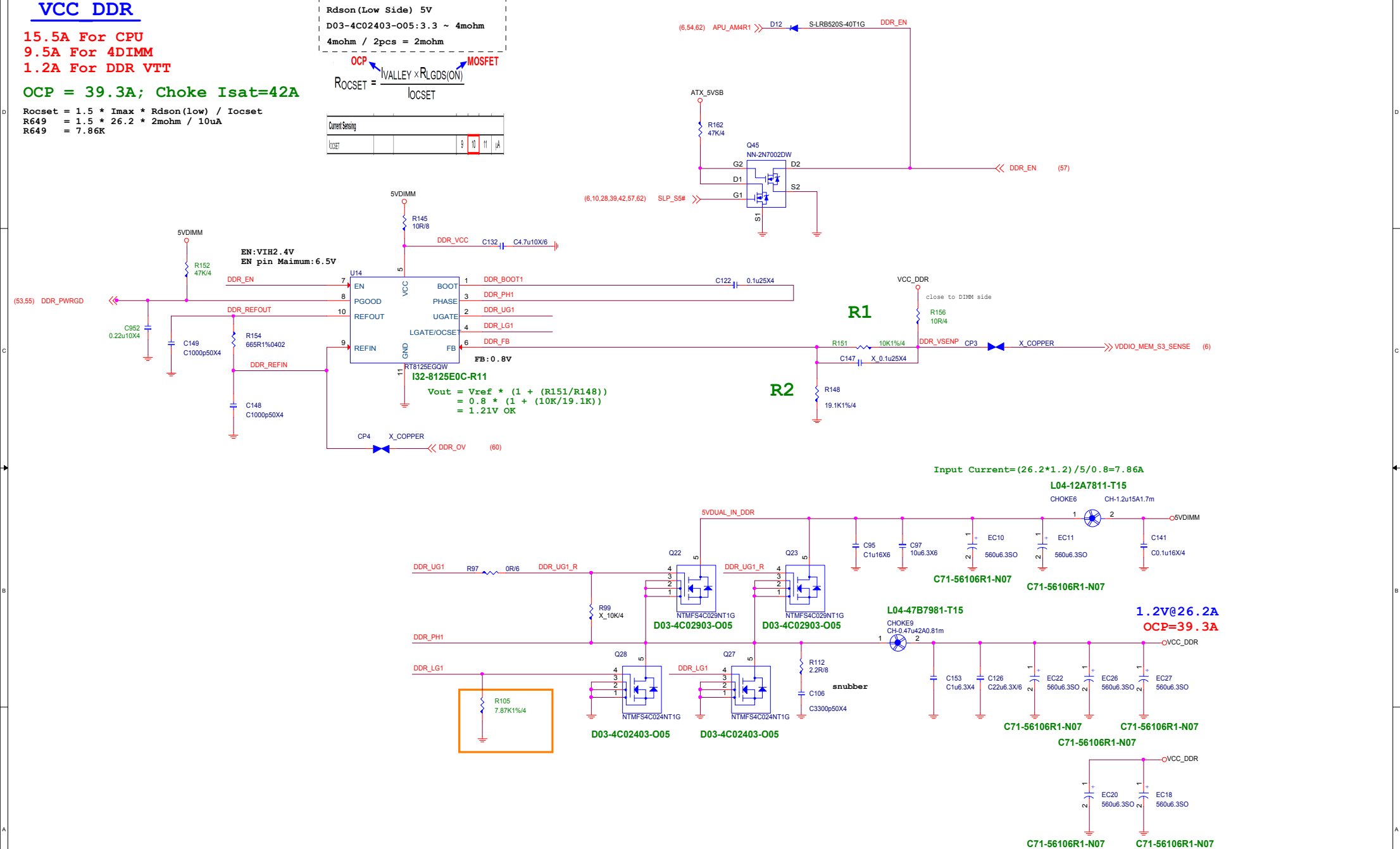
```
Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649   = 1.5 * 26.2 * 2mohm / 10uA
R649   = 7.86K
```

Rdson(Low Side) 5V
 D03-4C02403-005:3.3 ~ 4mohm
 4mohm / 2pcs = 2mohm

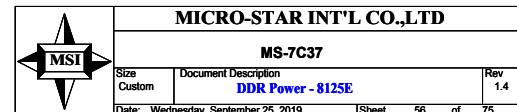
OCP \swarrow $I_{\text{VALLEY}} \times R_{\text{LGDS(ON)}}$ \searrow MOSFET

$$R_{\text{OCSET}} = \frac{I_{\text{VALLEY}} \times R_{\text{LGDS(ON)}}}{I_{\text{OCSET}}}$$

Current Sensing				
locset		9	10	11 μA



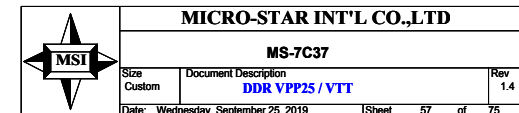
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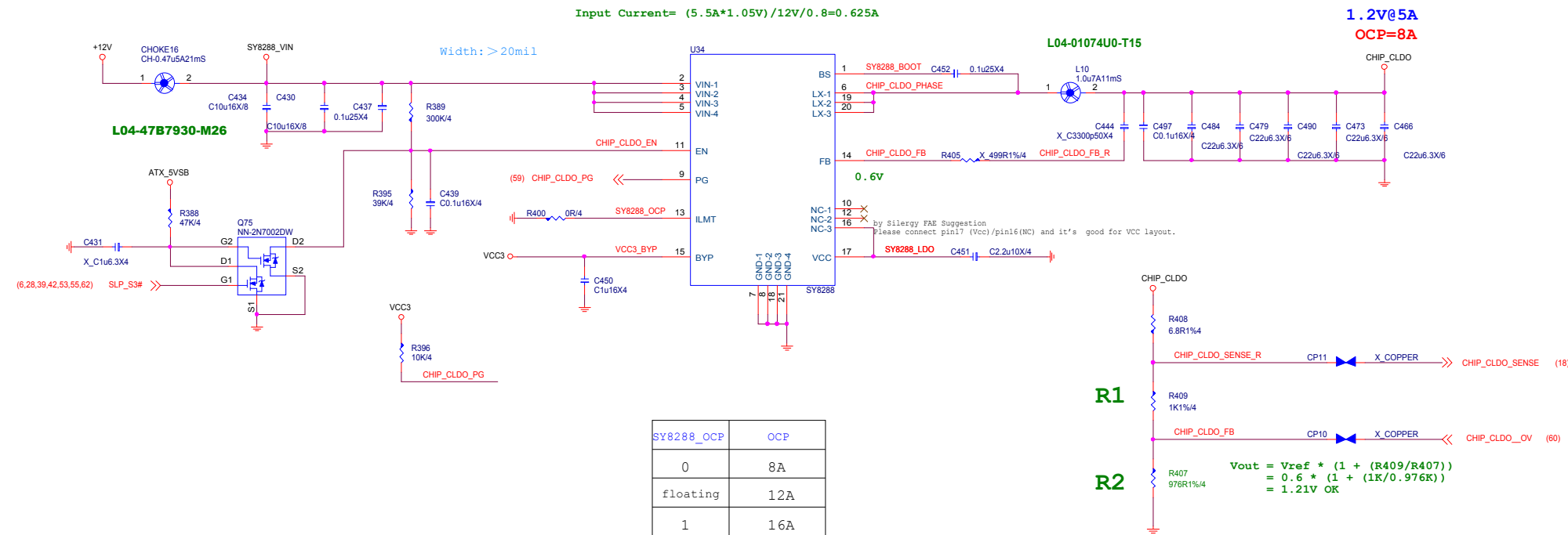
2.5V@2.24A



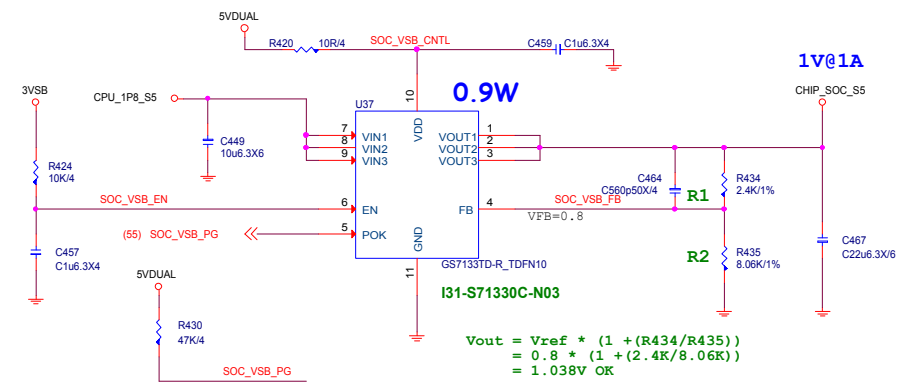
0.6V@1.2A



CHIP CLDO
CHIP: VDD_CLDO@5A

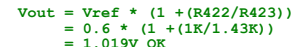


CHIP SOC S5
CHIP: VDDCR_SOC_S5@1A



CHIP: VDDCR_SOC@9A

```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH
```



The schematic shows the PM_PWROK signal path. It starts with three inputs: CHIP_SOC_POK (D39), CHIP_CLDO_PG (D41), and SYSREST# (D40). These are connected to S-LRB520S-40T1G comparators. The output of D41 is labeled (58) CHIP_CLDO_PG. The output of D40 is labeled (6,7,55,63) SYSREST#. The outputs of D39 and D41 are connected to the input of U73, NC7SZ08M5X, which is configured as an OR gate. The output of U73 is connected to R472 (1K/4) and then to the input of Q89, NN-2N7002DW, which is configured as a buffer. The output of Q89 is connected to the PM_PWROK pin (17).



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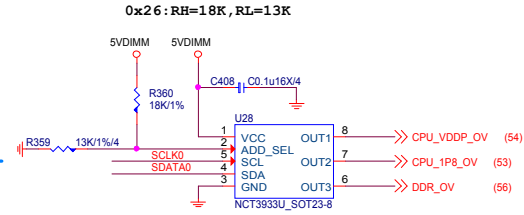
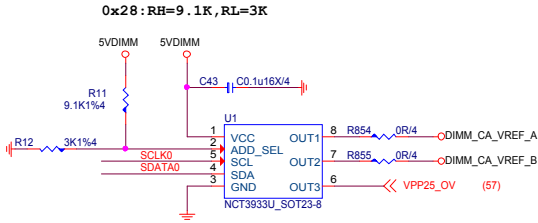
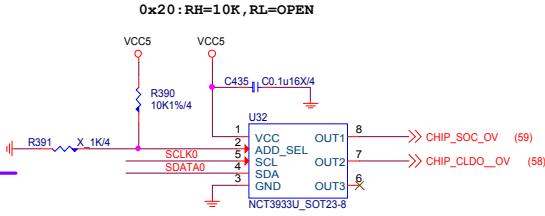
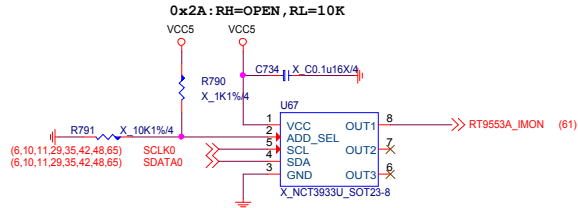
MS-7C37

Size Custom	Document Description PROM - NB503 / 1.0V	Rev 1.4
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Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

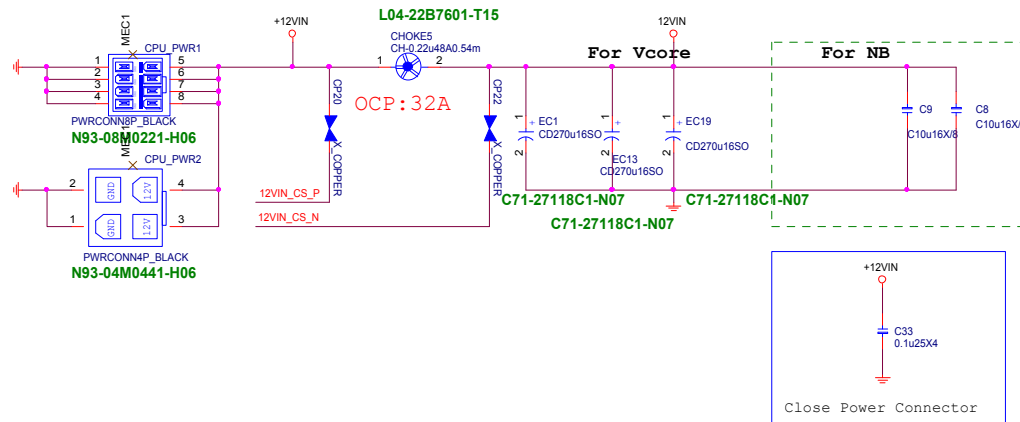


MICRO-STAR INT'L CO.,LTD

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Custom	OV Control - NCT3933	1.4
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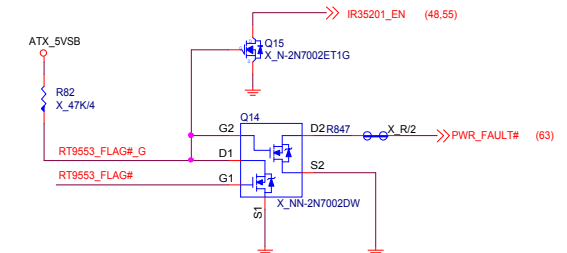
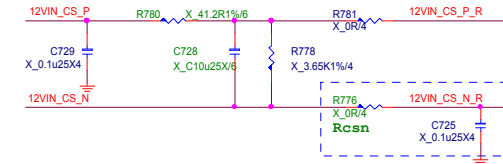
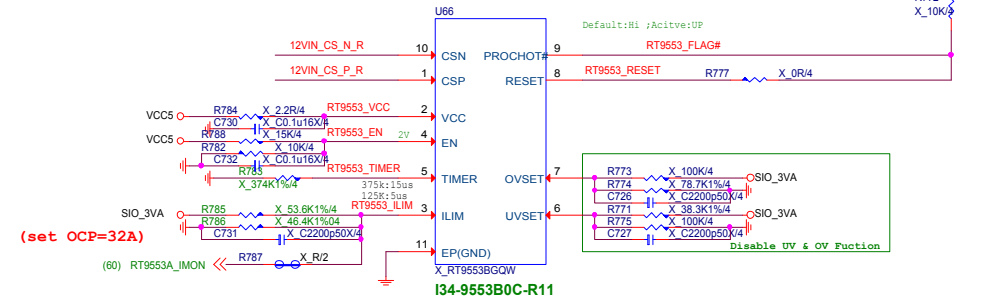
CPU POWER CONNECTOR



Vcore	SOC
$D = V_{out}/V_{in}$ $V_{in} = 12$ > input voltage $V_{out} = 2$ > output Vcore $D = 0.166667$	$D = V_{out}/V_{in}$ $V_{in} = 12$ > input voltage $V_{out} = 1.55$ > output Vcore $D = 0.129167$
$I_o = I_{core}(max)*0.8$ $I_{core}(max) = 200$ > Vcore current $I_{avg} = 160$ A	$I_o = I_{core}(max)*0.8$ $I_{core}(max) = 75$ > Vcore current $I_{avg} = 60$ A
$I_{ripple} = \{I_o * \sqrt{D} * \sqrt{(1-D)}\} / \text{Phase}$ $\text{Phase} = 10$ phase $I_{ripple} = 5.962848$ A	$I_{ripple} = \{I_o * \sqrt{D} * \sqrt{(1-D)}\} / \text{Phase}$ $\text{Phase} = 2$ phase $I_{ripple} = 10.06153$ A
How many pcs. Of Cap. $I_{ripple}(cap) = 4700$ mA $COE_{TEMP} = 1$ $\text{Input Cap.} = 2$ pcs.	How many pcs. Of Cap. $I_{ripple}(cap) = 4700$ mA $COE_{TEMP} = 1$ $\text{Input Cap.} = 3$ pcs.

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

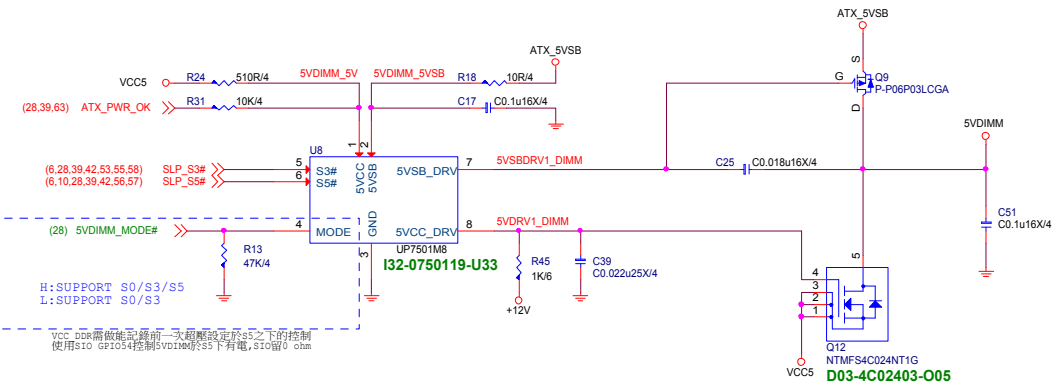


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Size Custom	Document Description OCF 12VIN - RT9533B	Rev 1.4
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5VDIMM FOR DDR



3VSB cost down

3.3V@3.363A

CPU: VDD_33_S5@0.25A

CHIP: VDD_33_S5@0.1A

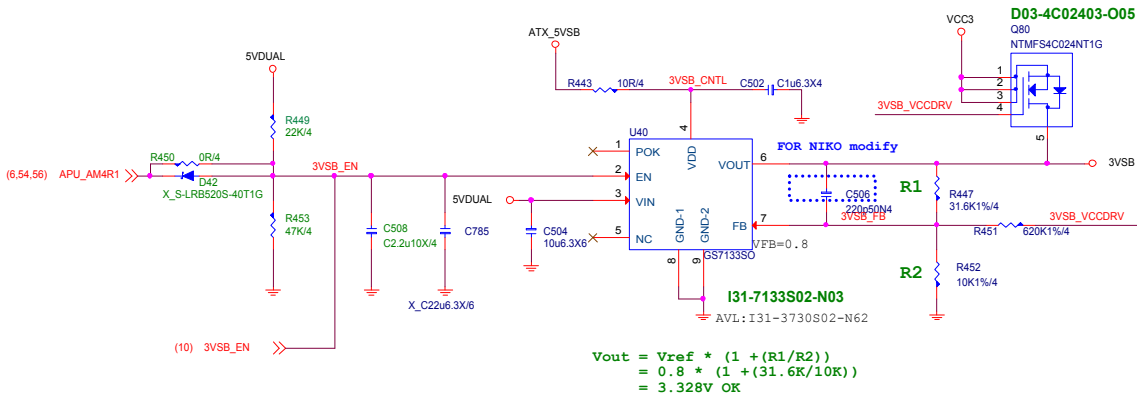
PCIE*4@1.5A

M.2 WIFI@0.78A

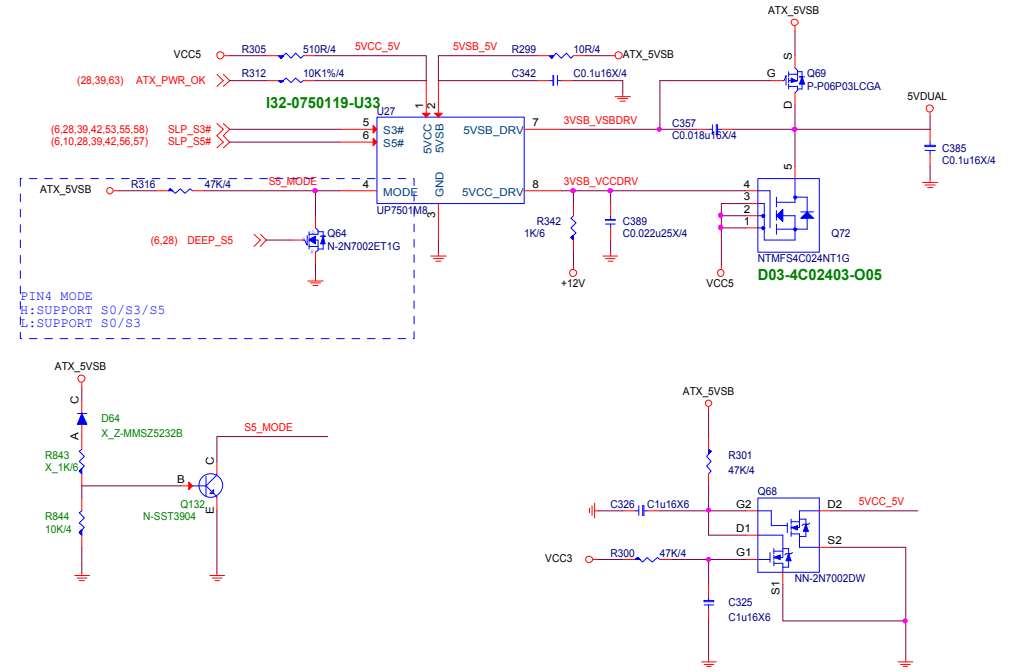
LAN@0.065A

Redriver*2@0.668A

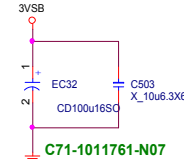
USB TYPE-C@0.9mA



5VDUAL For 3VSB、CPU 1.8V、VDDP



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

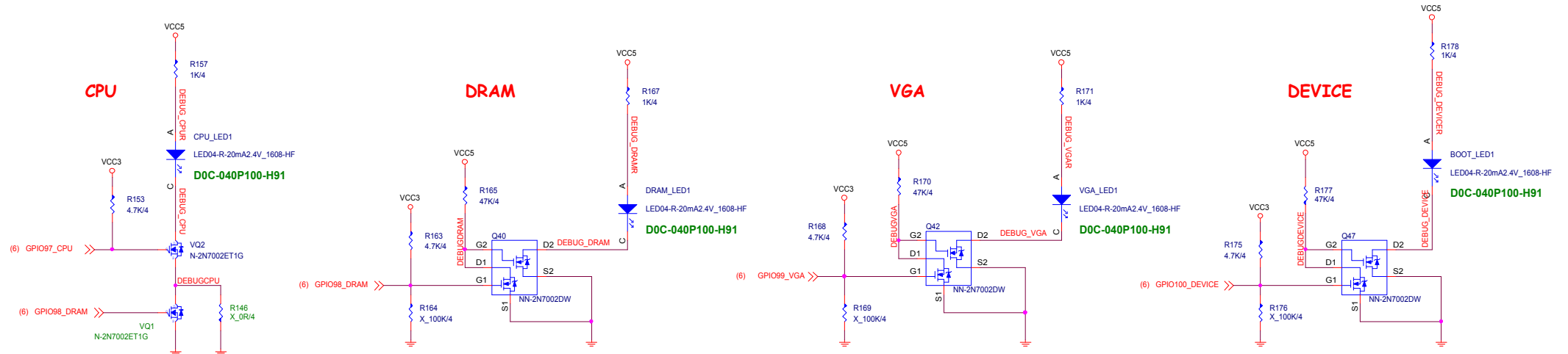


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Size	Document Description	Rev
Custom	ACPI - 3VSB / 5VDIMM	1.4
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EZ Debug LED



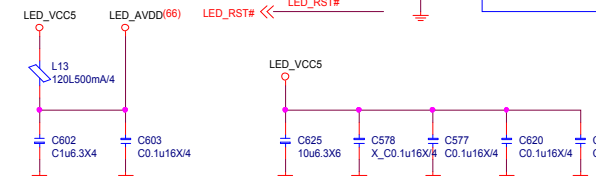
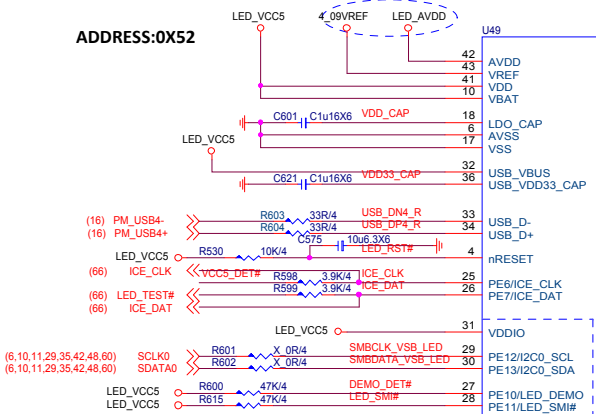
LED亮燈時同時將CPU LED關掉

LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

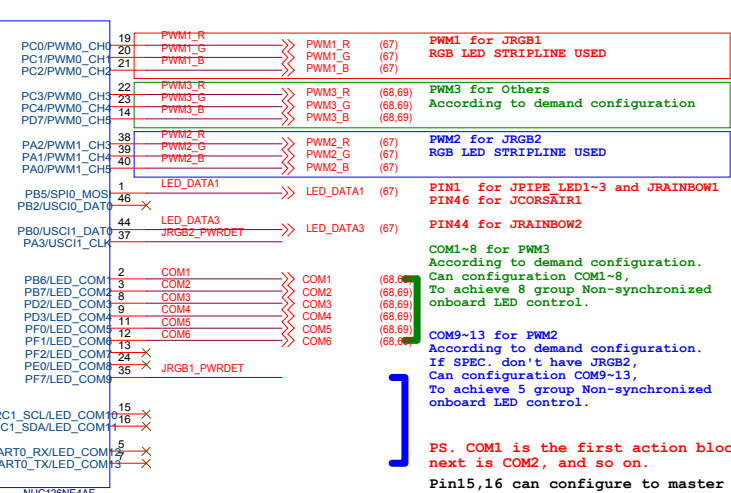
AMD AMP Detect LED

48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4 09VREF stuff for VREF.

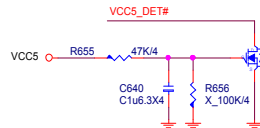


C1822 & C1823 near AVDD Pin.
C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB VBUS Pin.

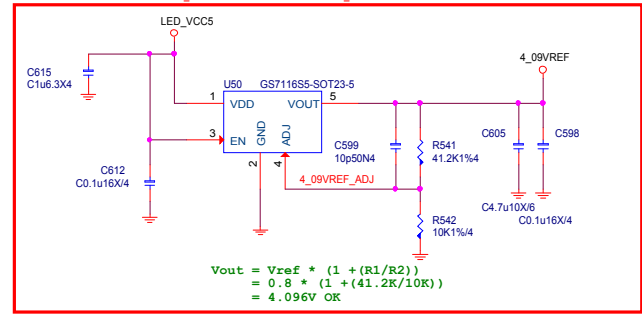
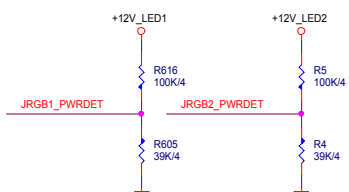
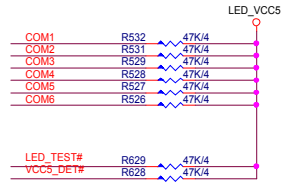
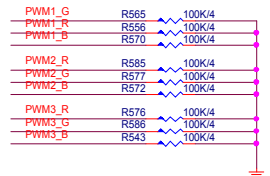


PS. COM1 is the first action block,
next is COM2, and so on.

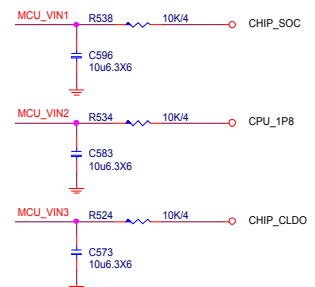
Pin15,16 can configure to master
smbus if spec requirement.



If SPEC has LED demo function without demo button,
DEMO_DET# must pull up to LED VCC5, Q319 need to stuff and control by LED_VCC5_EN.
PS. R630 remove, R600 and Q101 need to stuff

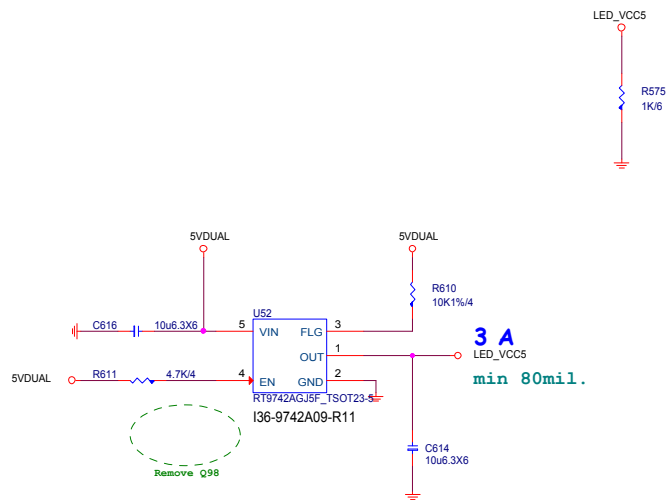


Option Spec For Voltage Monitor Require.



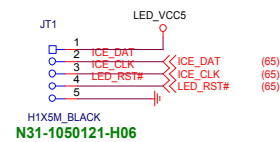
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

EXTERNAL POWER INPUT



External Power

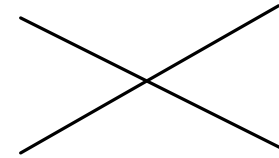
JT1 for FW update



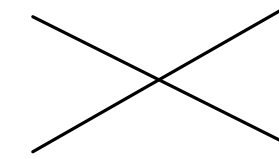
JF1 For Factory Test



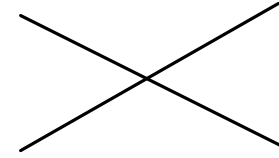
1 PCH HEATSINK LED



2 AUDIO/IO Cover LED



3 MOS HEATSINK LED



JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

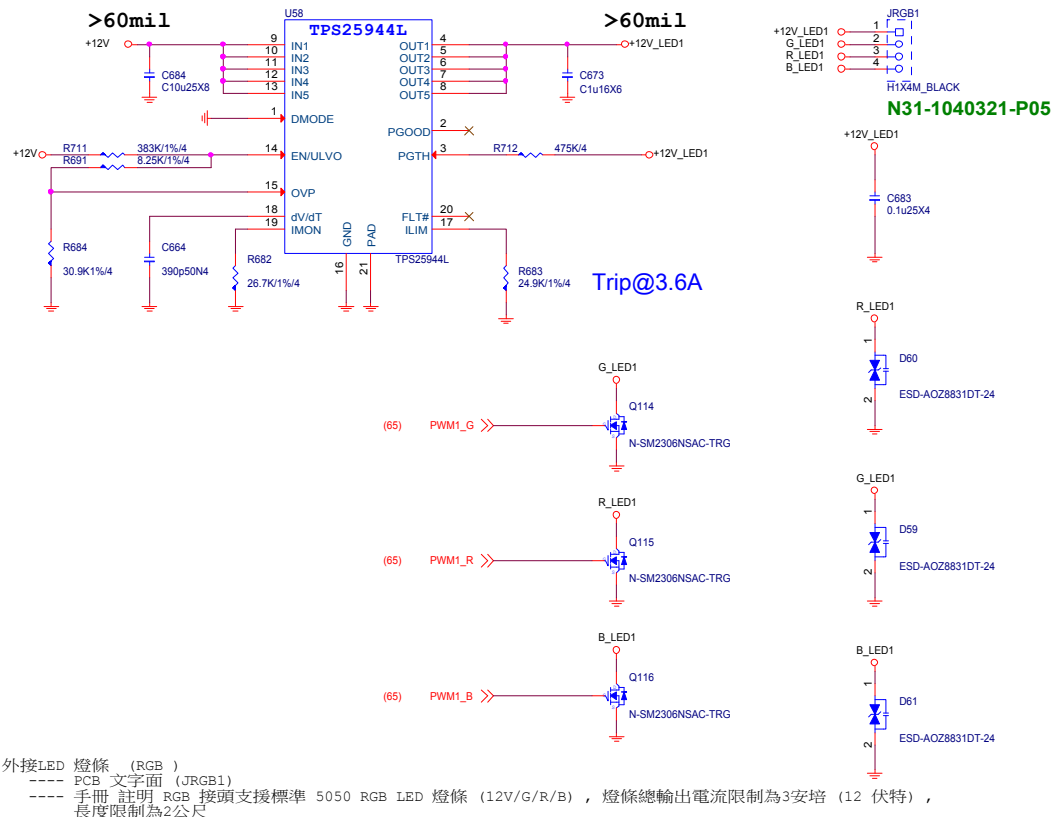


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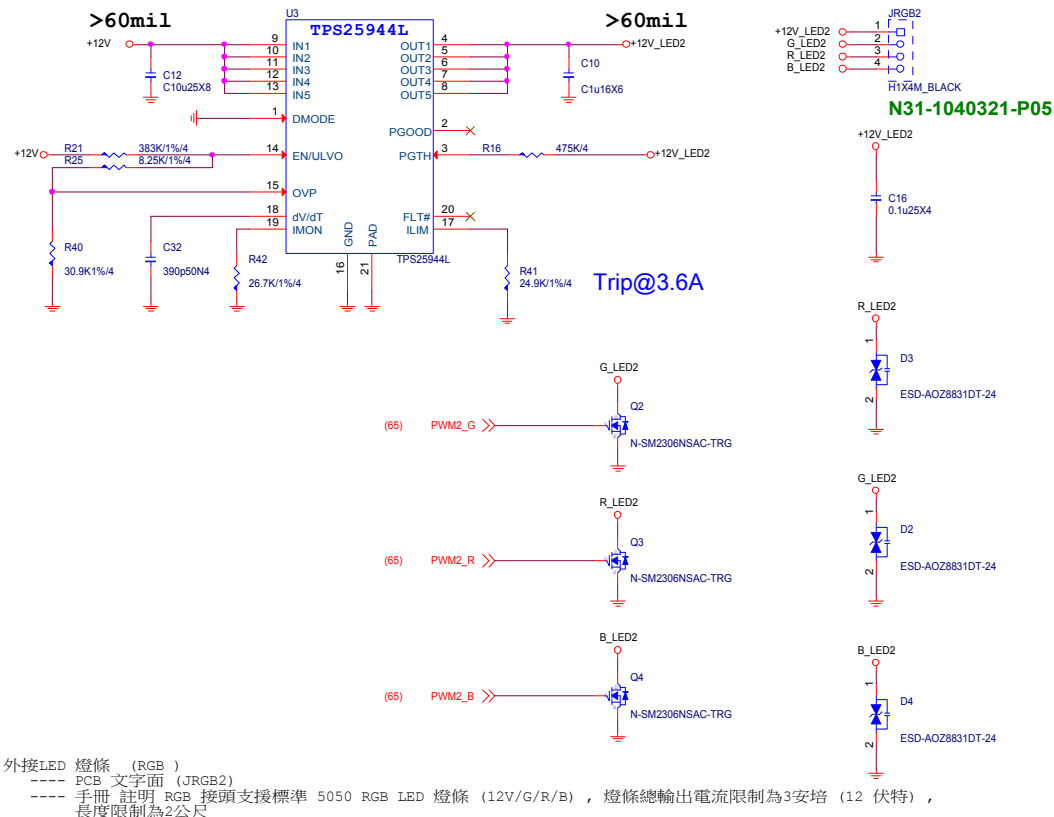
MS-7C37

Size Custom	Document Description LED - Power / JPIPE	Rev 1.4
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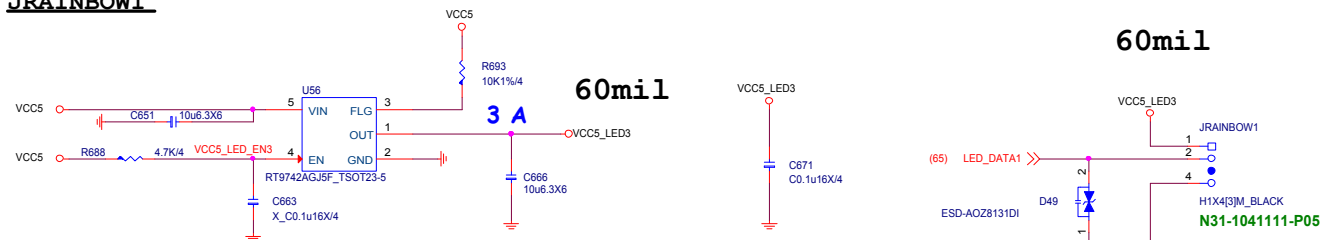
JRGB1



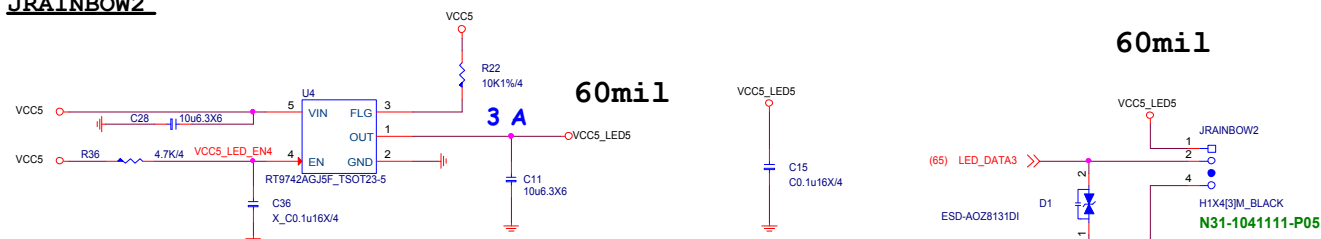
JRGB2



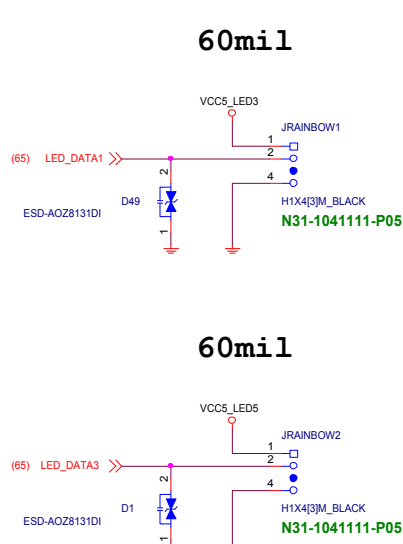
JRAINBOW1



JRAINBOW2

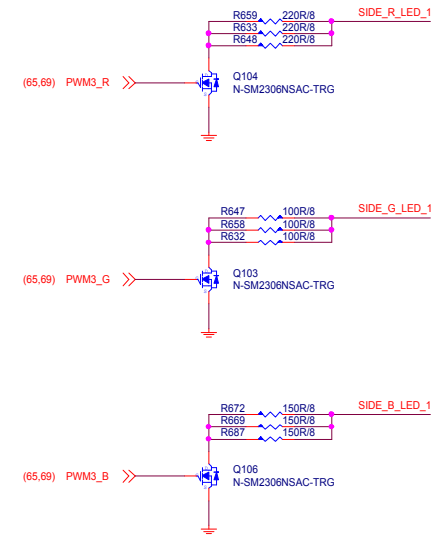
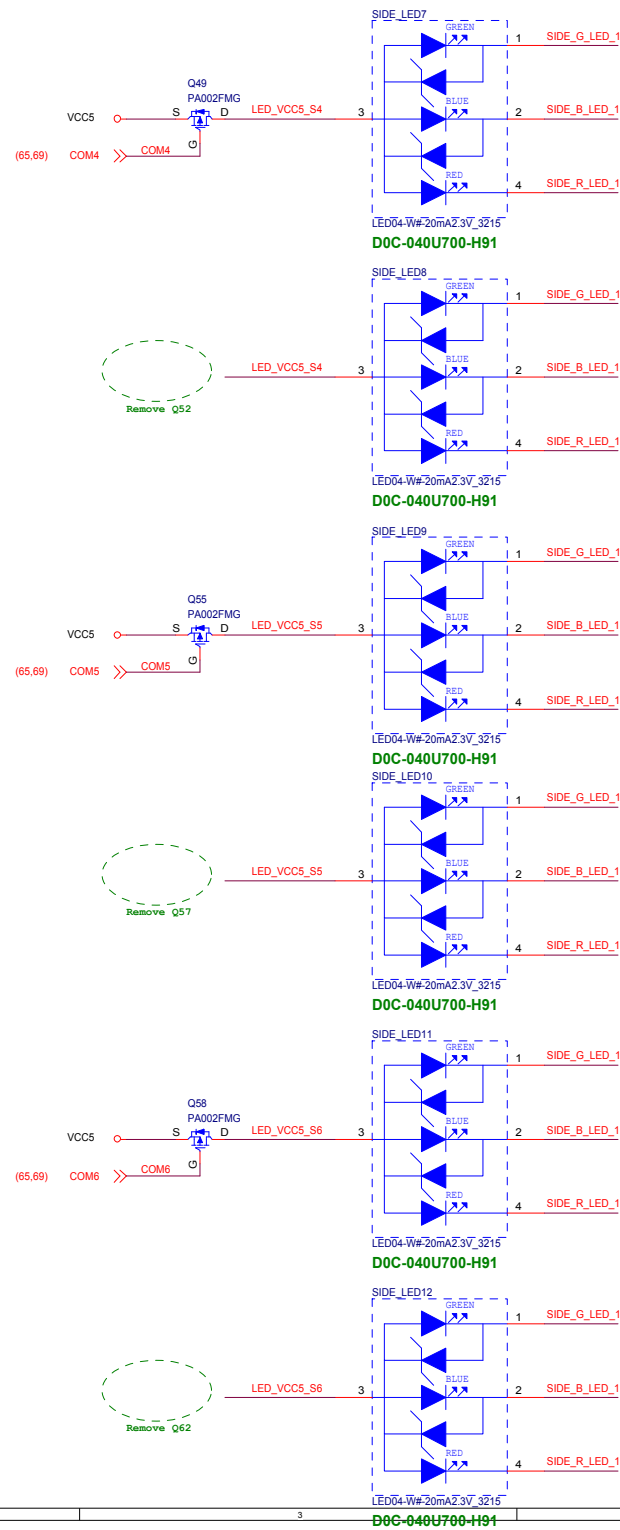
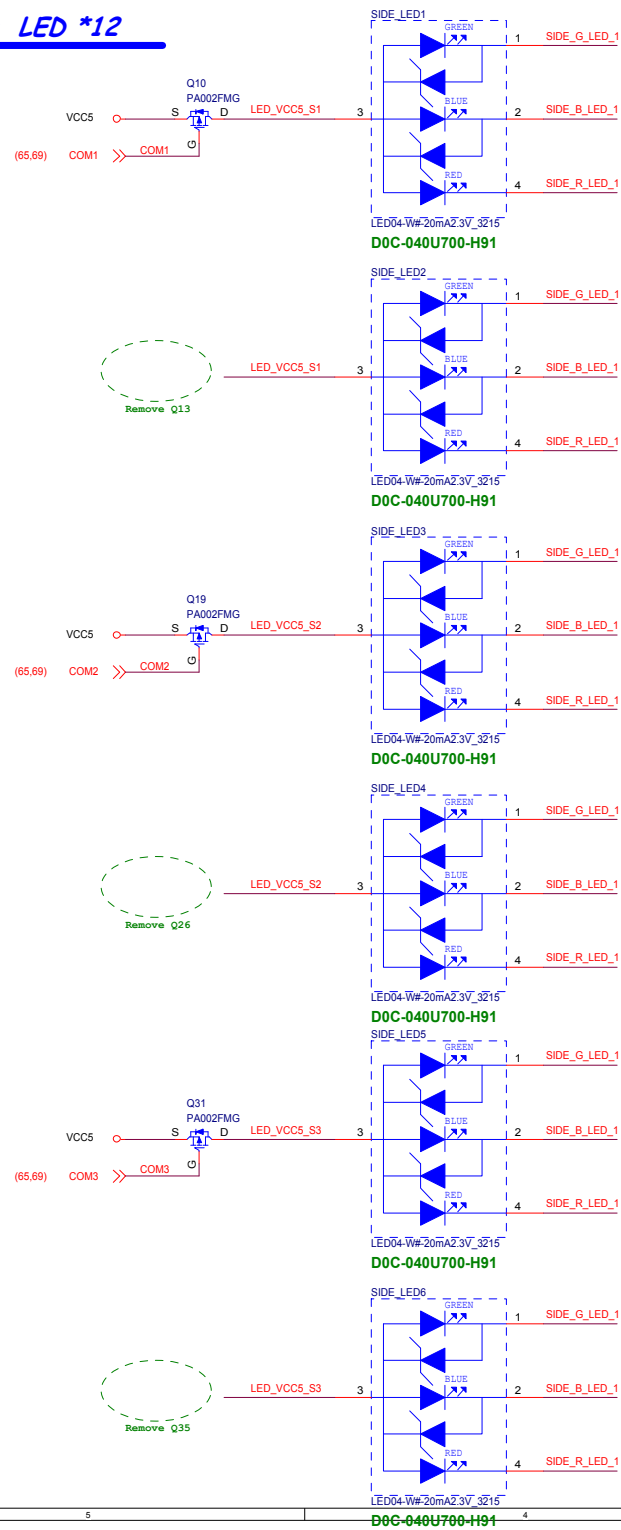


JCORAIR1



MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	LED - JLED1 / 2 / 3 / 4	1.4
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Sidebar LED *12

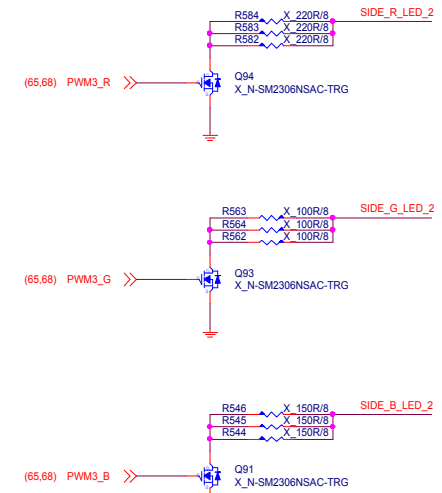
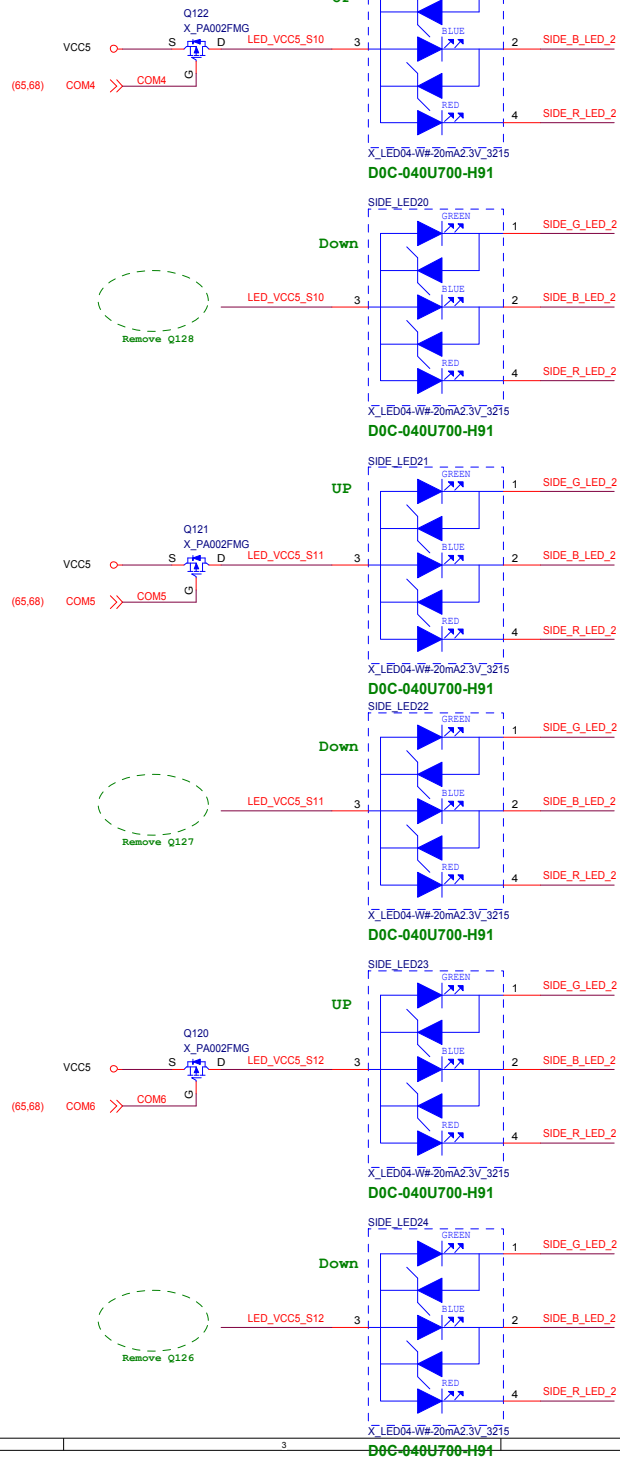
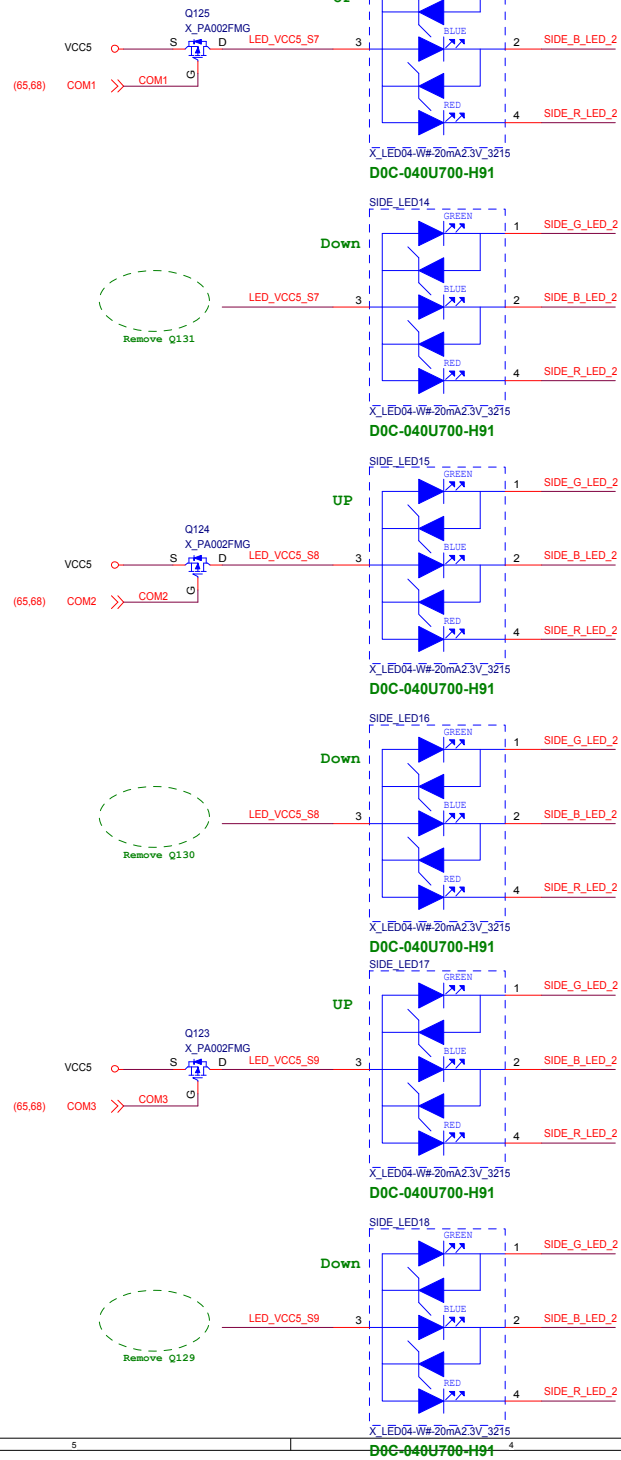


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Market Name LED *12

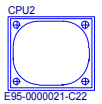


MICRO-STAR INT'L CO.,LTD

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CPU Socket



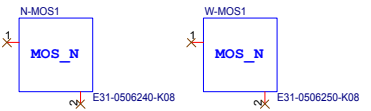
E95-0000022-C22

PCB



7C37-1.4
PD0-07C3714-E48

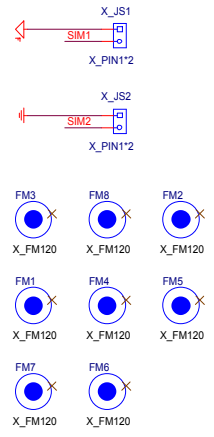
MOS HEATSINK



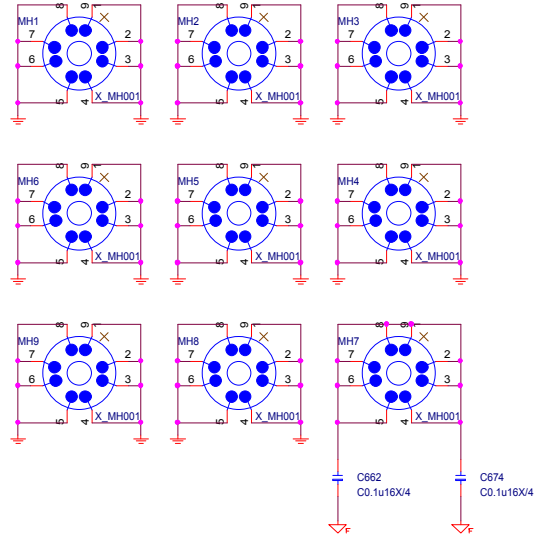
IO COVER



Simulation



Optics Orientation Holes



MANUAL PART

UEFI1
G51-MTSPXXA-A09
G51-M1SPXXA-A09

HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000

NAHIMIC1
Y02-MU00100-NAH
Y02-MU00100-NAH

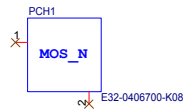
XSPILT1
X_Y02-MA00401-XSP
Y02-MA00401-XSP

SSE1
X_Y02-MA00101-SSE
Y02-MA00101-SSE

BAT1_XT
BAT-BCR2032P

AVL1:
D06-0100161-F52
D06-0100101-E26

PCH HEATSINK



Audio COVER



DDR COVER